

Dual Active Bridge Converter with PWM Control

In Solid State Transformer Application

by

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ABSTRACT

For the solid-state transformer (SST) application, a three-stage configuration consisting of a PWM rectifier based AC/DC stage, a dual active bridge (DAB) converter based DC/DC stage and a PWM inverter based DC/AC stage offers several advantages. For single-phase SST, the instantaneous input and load power seen by the DC/DC stage varies from zero to twice the load average power at double the line frequency. Traditionally, with phase-shift control, large DAB DC link capacitors are used to handle the instantaneous power variation of the load, with the DAB converter processing only the load average power resulting in better soft-switching range and consequently high efficiency. However, the large electrolytic capacitors required adversely affect the power density and the reliability of SST.

In this thesis, a PWM control is used for the DAB converter in SST, which extends the ZVS range of DAB and allows the DAB converter to handle the pulsating power while maintaining/improving efficiency. The impact of the output capacitance of switches with PWM control is discussed for practical implementation. A 40kHz, 500W DAB converter is designed and built, and the experimental results proves that the DAB converter with PWM control in SST can

achieve comparable efficiency while the DC link capacitors of SST can be reduced to a value that electrolytic capacitors are not required.

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Chapter 1. Introduction

1.1 Introduction to Solid-state Transformer

High frequency power electronics converter based solid-state transformer (SST) is gaining considerable attention as a key element of emerging smart distribution systems with numerous functionalities including reactive power control, voltage regulation, power quality and efficient interface for distributed generation and storage[1] [2]. By using the high frequency SST, the size and weight of distribution transformers can be significantly reduced compared to using the traditional bulky and heavy low frequency (60Hz in the US) transformer. Besides, the SST can achieve high efficiency that comparable to the old line-frequency transformer with state-of-the-art solid state devices, such as new generation SiC devices [3].

Among the various SST configurations, the three-stage SST consists of AC/DC PWM rectifier, DC/DC converter and DC/AC PWM inverter is a good choice due to its superior controllability that enable all SST functions, including reactive power control, power quality control, storage management, providing both high voltage and low voltage DC links and so on [4] [5]. For the DC/DC stage of SST, the dual active bridge converter (DAB) is preferred due to its simple structure, ZVS feature, and seamless bi-directional power flow capability. One

major challenge of DAB converter is to extend ZVS range and reduce transformer leakage rms current and consequently achieve high efficiency at light load [6].

The structure of a three-stage SST is shown in Fig. 1.1.

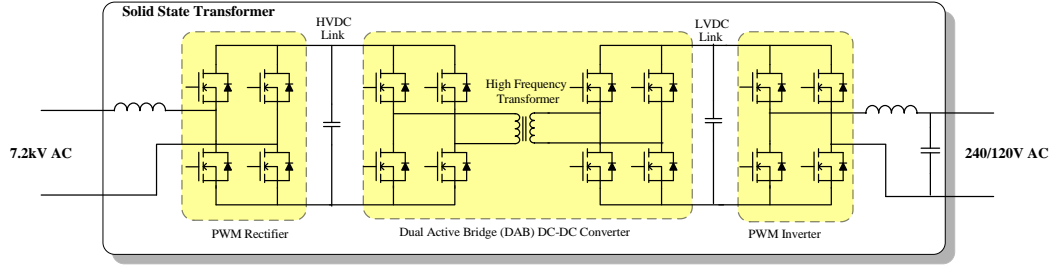


Fig. 1.1 Three-stage Solid-state Transformer

1.2 Thesis Objective and Outline

1.2.1 Thesis Objective

Due to the low efficiency of DAB converter with traditional phase-shift (PSM) control at light load, large DC link capacitors are required in SST handling double line frequency instantaneous power variation to make DAB converter process constant power and consequently obtain high conversion efficiency. However, the large electrolytic capacitors required adversely affect the power density and the reliability of the SST.

The objective of this thesis is to develop a new modulation method or select a proposed modulation method of DAB converter suitable for the solid-state transformer application so that the DC link capacitors can be reduced to a value

that electrolytic capacitors are not required while the efficiency of the converter is comparable with traditional phase-shift modulation and large DC link capacitors.

1.2.2 Outline

Chapter 2 describes the basic operation principles of DAB with traditional phase-shift control and analyzes the design issues of high frequency transformer in DAB converter. Lastly, the drawbacks of DAB converter are analyzed which indicates that a new modulation method is needed to address these problems.

Chapter 3 presents a comprehensive analysis of PWM control of DAB, including single PWM control of either input or output bridge at one time or simultaneous dual PWM control of both bridges. The basic operation principles are described. Furthermore, the design of high frequency transformer and the effect analysis of switch output capacitance for practical implementation are presented.

Chapter 4 gives an analysis about how extent the DC links capacitors can be reduced with PWM control of DAB. Based on available experiment condition, a 500W rated power DAB converter is designed, including power stage design and high frequency transformer and external leakage inductor designs. Then simulation and experiment results are shown to verify the objective of this thesis.

Chapter 5 is the conclusion of this thesis.

Chapter 2. Analysis of Dual Active Bridge

2.1 Introduction of Dual Active Bridge

For the DC/DC stage of solid-state transformer (SST), the dual active bridge (DAB) converter is preferred due to its simple structure, high power density, soft-switching feature, the capability of bi-directional power flow and easily implemented phase-shift (PSM) control. The circuit of DAB converter, shown in Fig. 2.1, consists of two voltage sourced full bridge DC-AC inverters that are connected to a high frequency isolation transformer. One huge advantage of DAB is that some parasitics in the circuit are used to achieve desirable properties. The leakage inductance of the high frequency transformer is used as the main energy transfer element and the output capacitance of switching devices is utilized to realize soft-switching operation [7] [8].

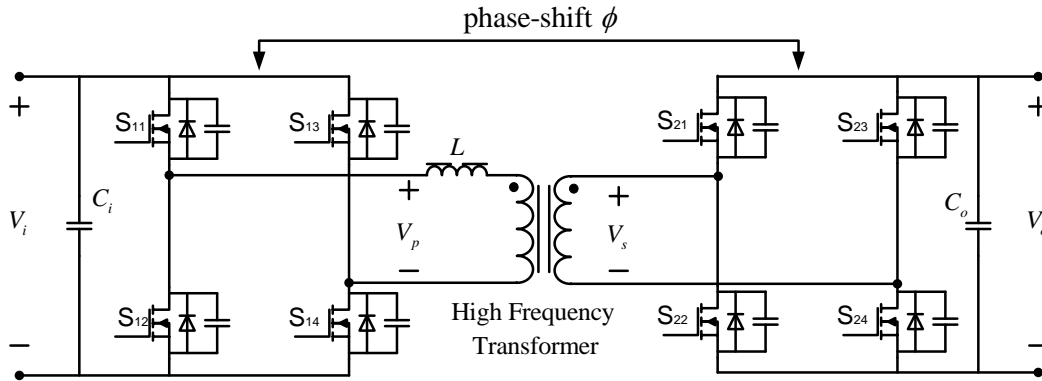


Fig. 2.1 Circuit of DAB Converter

2.2 Steady State Operation Analysis

To simplify the analysis, the primary-referred simplified equivalent circuit of DAB converter is shown in Fig. 2.2. It is assumed that: 1) all resistance is negligible; 2) transformer magnetizing inductance is neglected; 3) transformer winding capacitance is neglected. The transformer is replaced by the equivalent leakage inductance. The outputs of primary and secondary side full bridge DC-AC inverters are square waveforms with a constant duty ratio of 50%, which are generated by operating all switches with 50% duty ratio and turning on/off the diagonal switches in the same bridge at the same time. The phase-shift between primary and secondary bridges is ϕ , as analyzed below, which determines the amount of power transferred from leading bridge to lagging bridge.

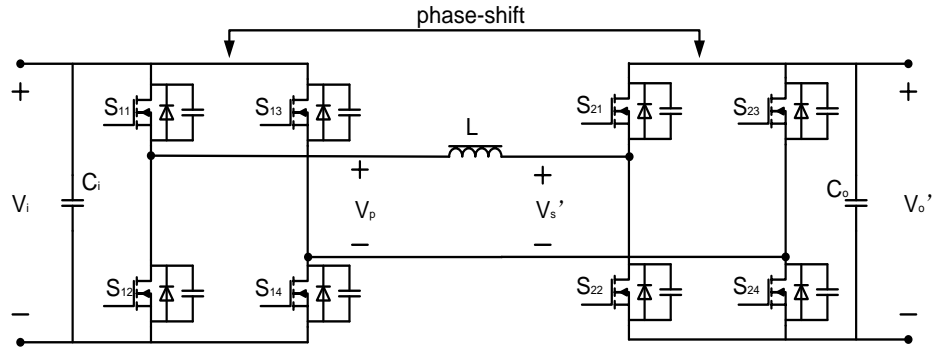


Fig. 2.2 Primary-referred Simplified Equivalent Circuit of DAB

2.2.1 Operation Principles

Fig. 2.3 shows the operation waveforms of DAB with both buck and boost modes for the forward power flow situation. For the transformer leakage

inductance current, the first and second half cycle waveforms are symmetric with respect to the horizontal axis (x axis). Regarding to the input and output currents, the second half cycle waveforms are the same as those of the first half cycle. Only first half cycle is therefore analyzed quantitatively hereinafter. From Fig. 2.3, it is clear that the leakage inductance current i_L is a function of $\theta = \omega t$, where ω is the switching angular frequency. Thus, the leakage inductance current expressions could be written and can be solved with symmetry condition.

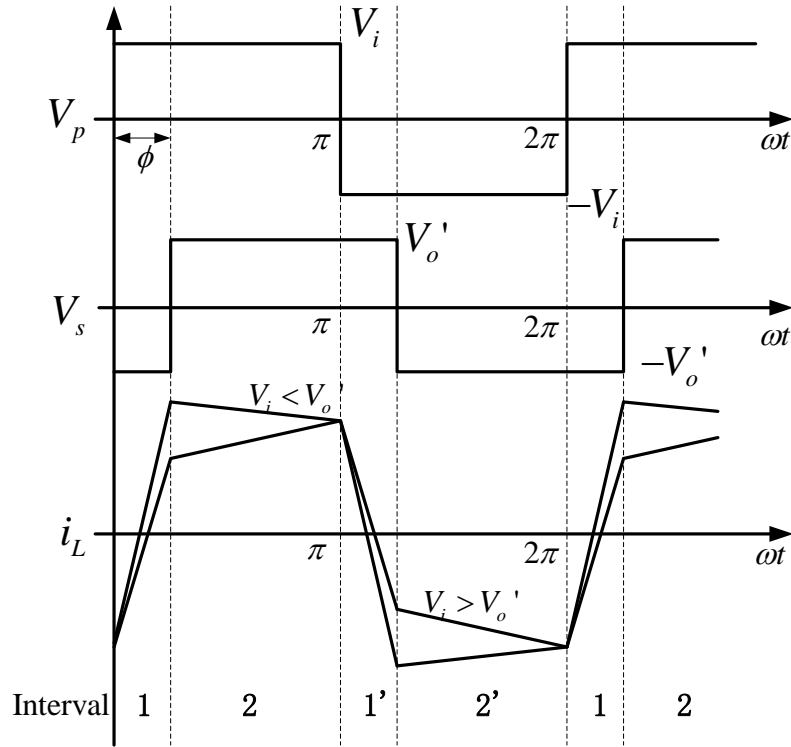


Fig. 2.3 Operation Waveforms of DAB with Buck and Boost Mode for Forward Power Flow Situation

Interval 1 ($0 \leq \theta < \phi$)

The operation circuits of Interval 1 are shown in Fig. 2.4(a) and (b); the only difference of these two Figures is the transformer leakage inductance current direction. In the interval 1, the transformer primary voltage $V_p(\theta) = V_i$ and primary-referred secondary voltage $V_s'(\theta) = -V_o'$, where V_o' is V_o/n and n is the transformer secondary to primary turns ratio. The current expression of interval 1 is therefore written as

$$i_L(\theta) = \frac{V_p(\theta) - V_s'(\theta)}{\omega L}(\theta - 0) + i_L(0) = \frac{V_i + V_o'}{\omega L} \cdot \theta + i_L(0) \quad \dots (2.1)$$

Transition from Inverter 1 to Interval 2

Fig. 2.4(c) and (d) shows the operation circuits of the transition from interval 1 to interval 2. The start of the transition is the turn-off of switch S_{23} and S_{22} while after which the stored inductive energy keeps the leakage inductance current flowing. In the transition, the initial voltages (at start point) across the output capacitance of S_{23} and S_{22} , C_{s23} and C_{s22} , are zero due to the previous on-state of both S_{23} and S_{22} (neglecting the voltage drop of the switch during on-state). On the contrary, the initial voltages of C_{s21} and C_{s24} are V_o' . In the transition, the leakage inductance current divides to two equal parts to discharge C_{s21} and C_{s24} and to charge C_{s23} and C_{s22} simultaneously, as shown in Fig. 2.4(c). Once the charging and discharging process is finished till the voltages of

C_{s21} and C_{s24} are zero while the voltages of C_{s23} and C_{s22} become V_o' , the current flows through the diode of S_{21} and S_{24} , D_{21} and D_{24} , as shown in Fig. 2.4(d). Then the switches S_{21} and S_{24} are turned on after a suitable dead time with zero-voltage switching. The switches' output capacitance and diode statuses are shown in Table 2.1.

Table 2.1 Transition Time Status (Interval 1 to Interval 2)

Transition Time			
C_{s21}	$V_o' \rightarrow 0$	D_{21}	off \rightarrow on
C_{s22}	$0 \rightarrow V_o'$	D_{22}	off
C_{s23}	$0 \rightarrow V_o'$	D_{23}	off
C_{s24}	$V_o' \rightarrow 0$	D_{24}	off \rightarrow on

Interval 2 ($\phi \leq \theta < \pi$)

Fig. 2.4(e) shows the operation circuit of interval 2. The transformer primary voltage $V_p(\theta) = V_i$ and primary-referred secondary voltage $V_s'(\theta) = V_o'$. The transformer leakage inductance current expression is written as

$$i_L(\theta) = \frac{V_p(\theta) - V_s'(\theta)}{\omega L} \cdot (\theta - \phi) + i_L(\phi) = \frac{V_i - V_o'}{\omega L} \cdot (\theta - \phi) + i_L(\phi) \quad \dots (2.2)$$

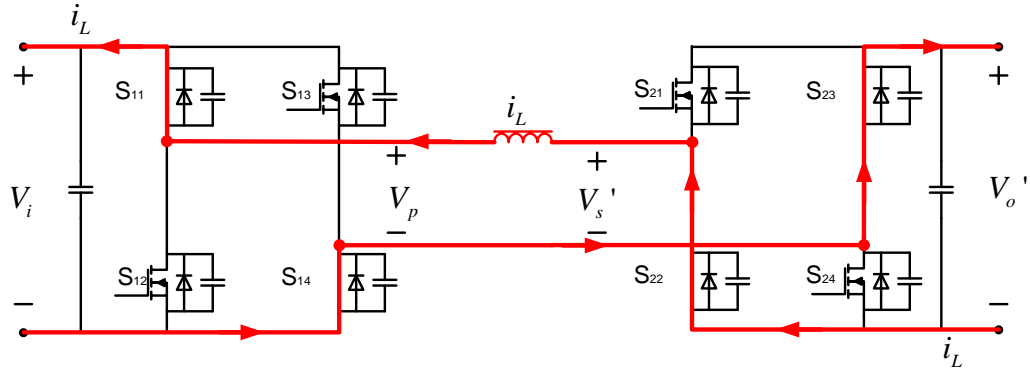
Transition From Interval 2 to Interval 1'

The transition circuits from Interval 2 to Interval 1' are shown in Fig. 2.4(f) and (g). Similar as the transition from Interval 1 to Interval 2, the discharging and

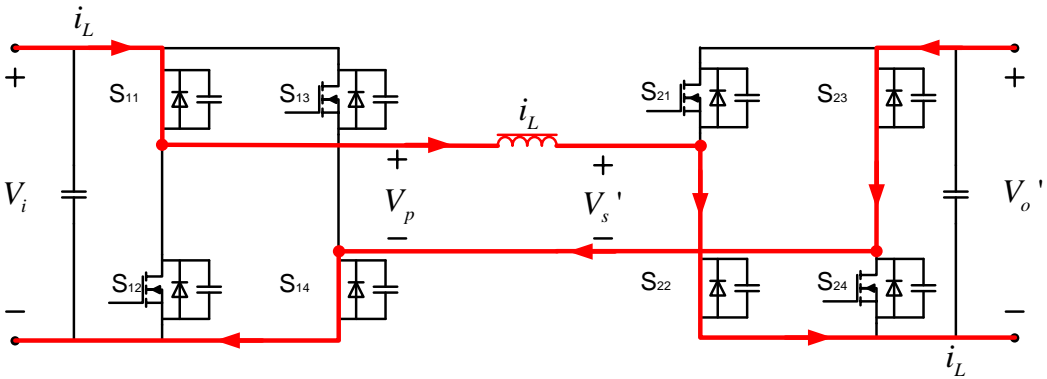
charging procedure occurs in input bridge instead of output bridge. The status changes are summarized in Table 2.2.

Table 2.2 Transition Time Status (Interval 2 to Interval 1')

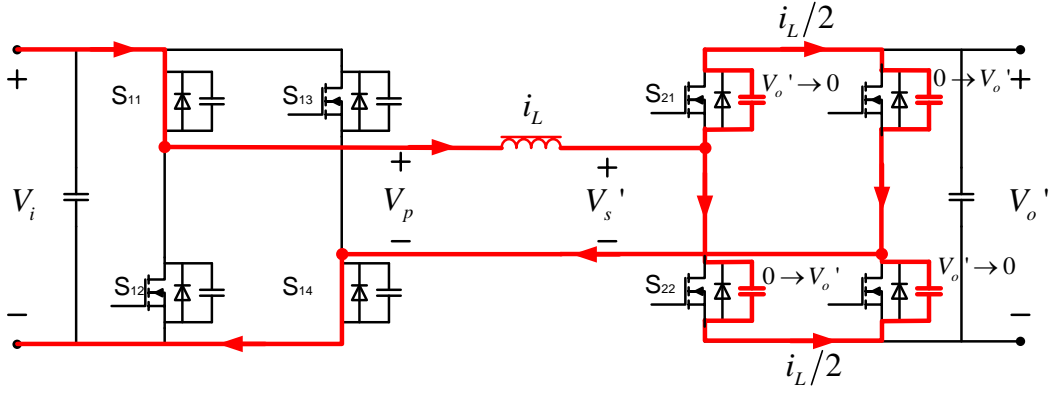
Transition Time			
C_{s11}	$0 \rightarrow V_o'$	D_{11}	off
C_{s12}	$V_o' \rightarrow 0$	D_{12}	off \rightarrow on
C_{s13}	$V_o' \rightarrow 0$	D_{13}	off \rightarrow on
C_{s14}	$0 \rightarrow V_o'$	D_{14}	off



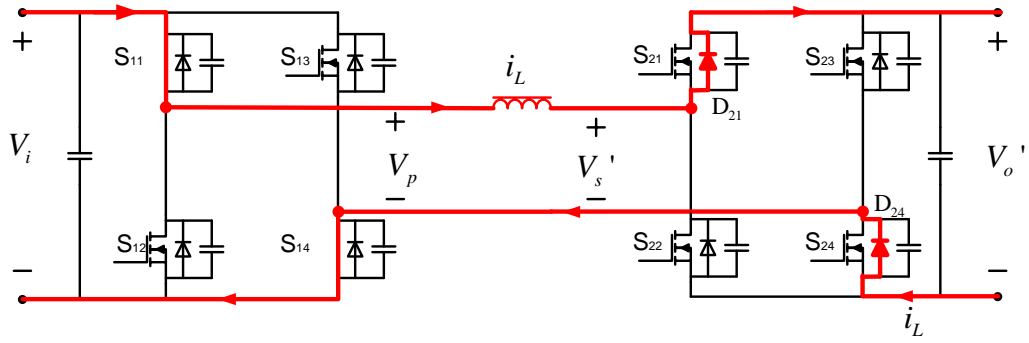
(a) Interval 1



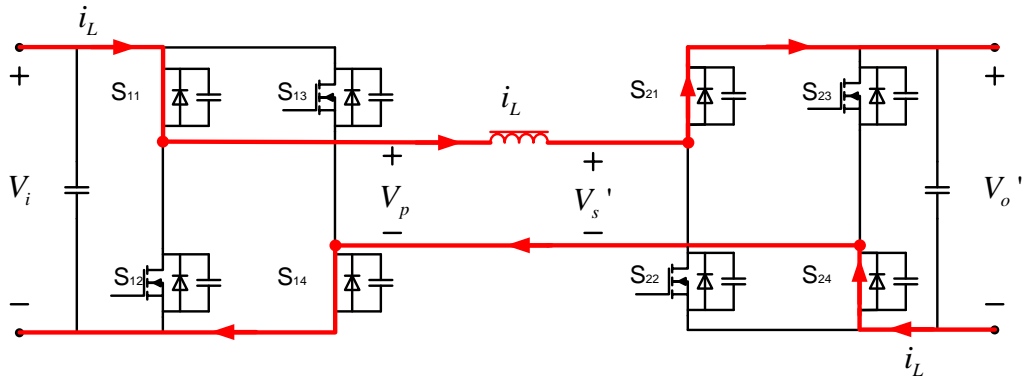
(b) Interval 1



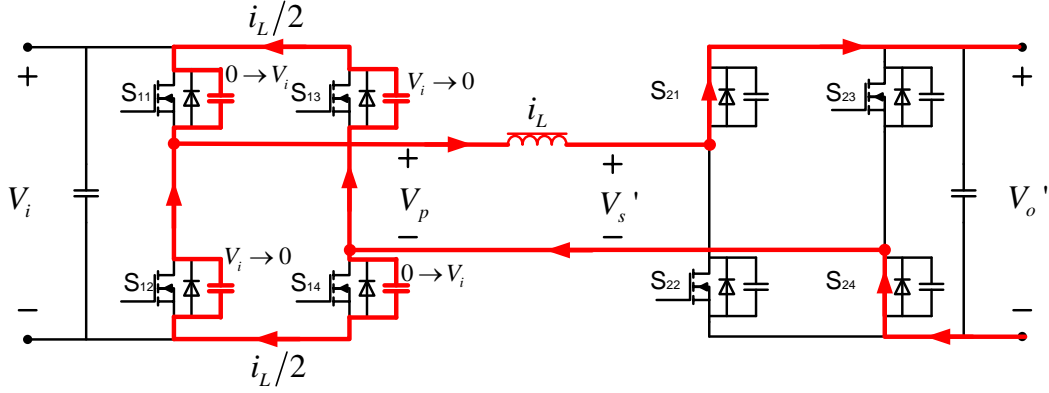
(c) Transition from Interval 1 to Interval 2



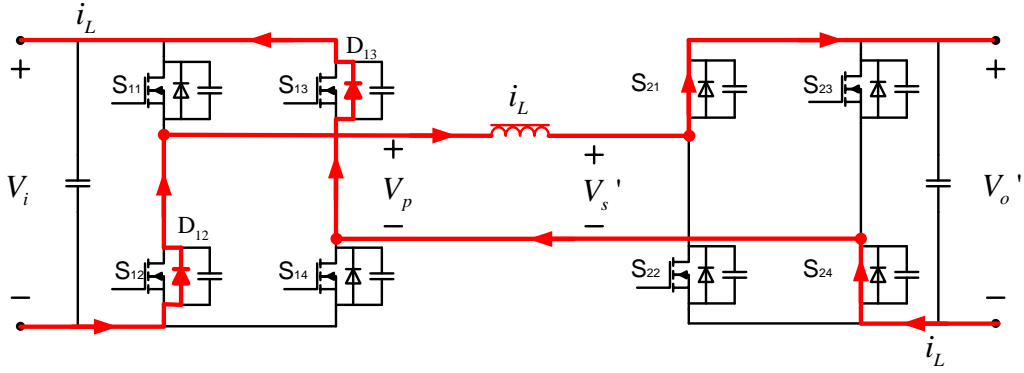
(d) Transition from Interval 1 to Interval 2



(e) Interval 2



(f) Transition from Interval 2 to Interval 1'



(g) Transition from Interval 2 to Interval 1'

Fig. 2.4 Steps of DAB Converter Operation Procedure

With symmetry condition $i_L(\pi) = -i_L(0)$, from eqn. (2.1) and eqn. (2.2), the transformer leakage inductance current expression at $\theta=0$ and $\theta=\phi$ can be solved as

$$i_L(0) = -\frac{V_i}{\omega L} \left[d\phi + \frac{\pi(1-d)}{2} \right] \quad \dots (2.3)$$

$$i_L(\phi) = \frac{V_i}{\omega L} \left[\phi - \frac{\pi(1-d)}{2} \right] \quad \dots (2.4)$$

where $d = \frac{V_o}{V_i}$. From Fig. 2.3, the primary-referred average output current is

$$i_{o,avg} = \frac{\frac{-(i_L(0) + i_L(\phi))}{2} \cdot \phi + \frac{i_L(\phi) + i_L(\pi)}{2} \cdot (\pi - \phi)}{\pi} = \frac{V_i}{\omega L} \cdot \frac{\phi(\pi - \phi)}{\pi} \quad \dots (2.5)$$

Thus the output power is derived as below,

$$P_o = i_{o,avg} \cdot V_o = \frac{V_i^2}{\omega L} \cdot d\phi \cdot \left(1 - \frac{\phi}{\pi}\right) \quad (0 \leq \phi \leq \pi/2) \quad \dots (2.6)$$

It is clear that the value of ϕ determines the output power of DAB converter, as shown in Fig. 2.5. It should be noted that this power equation is derived based on forward power flow situation. Considering the symmetry of the circuit, a similar analysis as in Section 2.2.1 for reverse power flow situation ($-\pi/2 \leq \phi \leq 0$) is done which shows that the power equation is

$$P_o = i_{o,avg} \cdot V_o = \frac{V_i^2}{\omega L} \cdot d\phi \cdot \left(1 - \frac{-\phi}{\pi}\right) \quad (-\pi/2 \leq \phi \leq 0) \quad \dots (2.7)$$

In summary, combine eqn. (2.6) and eqn. (2.7), for both forward and reverse power flow, the power transferred by DAB converter is

$$P_o = \frac{V_i^2}{\omega L} \cdot d\phi \cdot \left(1 - \frac{|\phi|}{\pi}\right) \quad (-\pi/2 \leq \phi \leq \pi/2) \quad \dots (2.8)$$

2.2.2 Soft-switching Constraints

From the transition analysis above, to realize zero-voltage switching of leading bridge (input bridge for forward power flow), at $t=0$ point, some energy stored in the leakage inductance is required, presented as leakage inductance

current, to charge and discharge switch output capacitance in leading bridge.

Therefore,

$$i_L(0) \leq 0 \quad \dots (2.9)$$

Combined eqn. (2.9) with eqn. (2.3),

$$d \leq \frac{1}{1-2\phi/\pi} \quad (0 \leq \phi \leq \pi/2) \quad \dots (2.10)$$

$$\phi \geq \frac{\pi(d-1)}{2d} \quad (0 \leq d \leq \infty) \quad \dots (2.11)$$

Regarding to the lagging bridge (input bridge for forward power flow), to achieve zero-voltage switching operation, the transformer leakage inductance current must be positive,

$$i_L(\phi) \geq 0 \quad \dots (2.12)$$

Substituting eqn. (2.12) in eqn. (2.4),

$$d \geq \frac{\pi-2\phi}{\pi} \quad (0 \leq \phi \leq \pi/2) \quad \dots (2.13)$$

$$\phi \geq \frac{\pi(1-d)}{2} \quad (0 \leq d \leq \infty) \quad \dots (2.14)$$

Eqn. (2.11) shows that, when d is greater than one, there is a requirement of minimum ϕ to achieve zero-voltage switching of leading bridge; for d is less than one situation, the leading bridge is always in soft-switching region. Also, eqn. (2.14) indicates that there is a requirement of minimum ϕ to realize zero-voltage switching of lagging bridge on the condition that d is less than one; When d is greater than one, the lagging bridge can always achieve

soft-switching. It should be noted when d is equal to one, there is no minimum requirement of ϕ . Considering that ϕ is directly related to the power transferred in the converter (as shown in eqn. (2.6)), when d is not equal to one, there is a minimum power requirement for soft-switching operation.

In addition, the similar analysis for reverse power flow situation shows the same conclusion as above regarding to the soft-switching region for both leading and lagging bridges. The above analysis is summarized in Table 2-3 as below. Also, Fig. 2.5 shows the output power versus phase-shift which is a graph type presenting eqn. (2.8) and Table 2.3.

Table 2.3 Soft-switching Constraints

	Forward Mode	Reverse Mode	$d < 1$	$d > 1$	$d = 1$
Leading Bridge	Input Bridge	Output Bridge	always	$ \phi \geq \frac{\pi(d-1)}{2d}$	always
Lagging Bridge	Output Bridge	Input Bridge	$ \phi \geq \frac{\pi(1-d)}{2}$	always	always

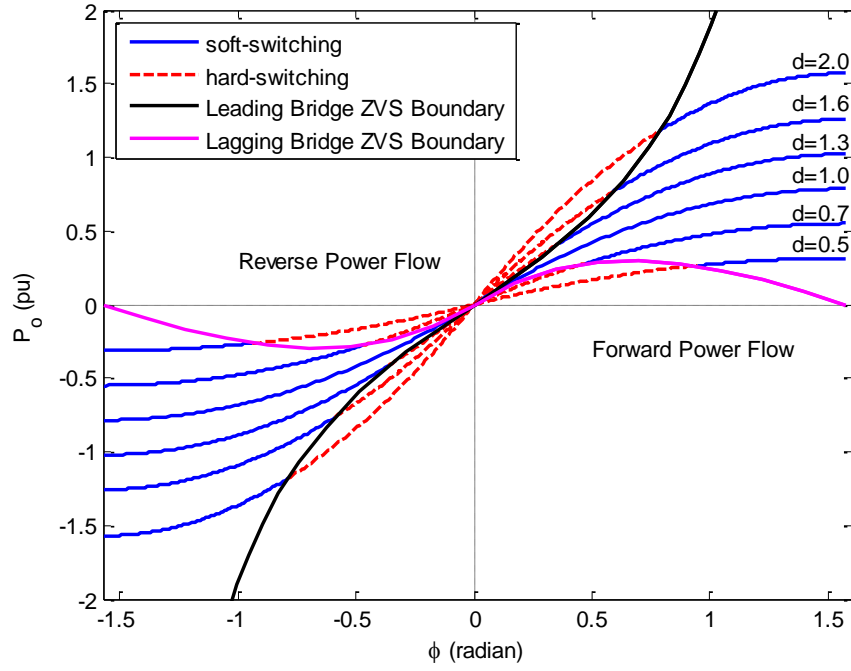


Fig. 2.5 Output Power versus Phase-shift

2.3 High Frequency Transformer Design Analysis

According to the Faraday's Law, the voltage across the transformer winding is

$$e(t) = N \frac{d\phi(t)}{dt} = N A_c \frac{dB(t)}{dt} \dots \quad (2.15)$$

where N is the winding turns and A_c is the cross-sectional core area. Thus the volt-second applied to the transformer winding is

$$e(t) \cdot dt = N \cdot A_c \cdot B_{\max} \dots \quad (2.16)$$

Buck Mode

When buck mode, as shown in Fig. 2.6(a), the maximum positive volt-second applied to winding is

$$\text{volt-second} = (V_i + V_o') \cdot \frac{\phi}{2\pi} \cdot T_s + (V_i - V_o') \cdot \frac{\pi - \phi}{2\pi} \cdot T_s \quad \dots (2.17)$$

It gets maximum value when $\phi = \phi_{\max} = \frac{\pi}{2}$ and thus

$$\text{volt-second}_{\max} = \frac{V_i + V_o'}{4} \cdot T_s + \frac{V_i - V_o'}{4} \cdot T_s = \frac{V_i}{2} \cdot T_s \quad \dots (2.18)$$

Boost Mode

When Boost Mode, as shown in Fig. 2.6(b), the maximum positive volt-second is

$$\text{volt-second} = (V_i + V_o') \cdot \frac{\phi}{2\pi} \cdot T_s + (V_o' - V_i) \cdot \frac{\pi - \phi}{2\pi} \cdot T_s \quad \dots (2.19)$$

Substitute $\phi = \phi_{\max} = \frac{\pi}{2}$ into eqn. (2.19),

$$\text{volt-second}_{\max} = \frac{V_o'}{2} \cdot T_s = \frac{dV_i}{2} \cdot T_s = \frac{V_o'}{2} \cdot T_s \quad \dots (2.20)$$

It should be noted that therefore the possible maximum volt-second for the DAB transformer is $\max\{V_i, V_o'\}/2 \cdot T_s$.

The apparent power P_t is a key parameter we need to know to design transformer due to its relationship with the geometry of the transformer---- A_p , if A_p design method is used [9] [10].

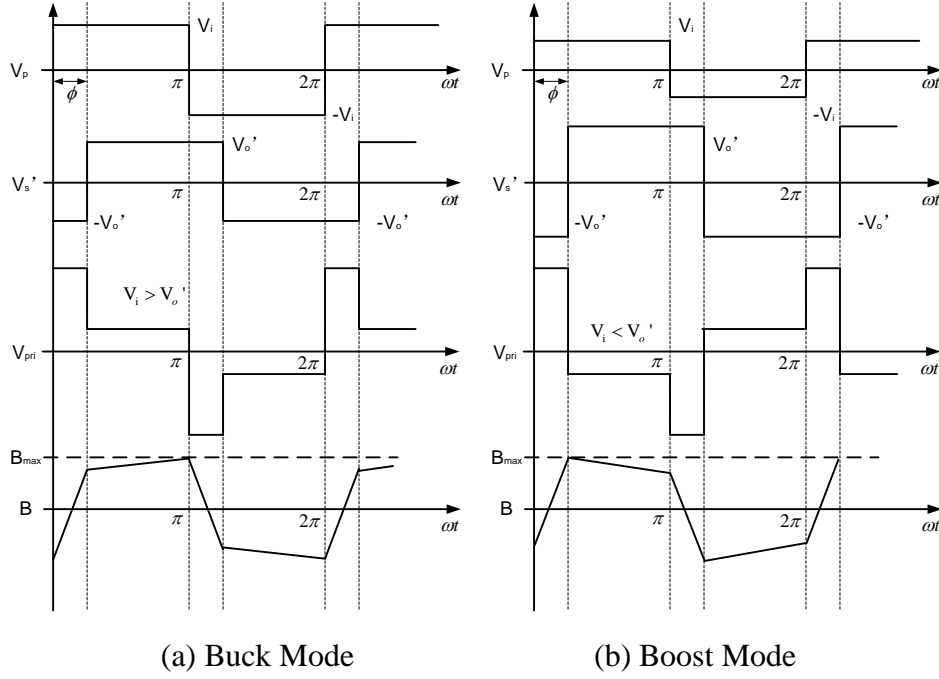


Fig. 2.6 Voltage and Flux Density Waveforms for Both Buck and Boost Modes

From eqn. (2.16) and eqn. (2.20), the primary and secondary turns can be expressed as:

$$N_{pri} = \frac{\max\{V_i, V_o'\}/2}{A_c \cdot B_{max} \cdot f_{sw}} \quad \dots (2.21)$$

$$N_{sec} = n \cdot \frac{\max\{V_i, V_o'\}/2}{A_c \cdot B_{max} \cdot f_{sw}} \quad \dots (2.22)$$

And assume the primary and secondary windings have equal current density J_m ,

$$K_u \cdot W_a = N_{pri} \cdot \frac{I_{Lrms}}{J_m} + N_{sec} \cdot \frac{I_{Lrms}/n}{J_m} \quad \dots (2.23)$$

where K_u is the utilization factor, W_a is the winding area, I_{Lrms} is the primary-referred transformer leakage inductance rms current, and J_m is the current density.

Substitute eqn. (2.21) and eqn. (2.22) into eqn. (2.23),

$$K_u \cdot W_a = \frac{\max\{V_i, V_o\}/2}{A_c \cdot B_{\max} \cdot f_{sw}} \cdot \frac{I_{Lrms}}{J_m} + n \cdot \frac{\max\{V_i, V_o\}/2}{A_c \cdot B_{\max} \cdot f_{sw}} \cdot \frac{I_{Lrms}/n}{J_m} = \frac{\max\{V_i, V_o\} \cdot I_{Lrms}}{A_c \cdot B_{\max} \cdot f_{sw} \cdot J_m} \dots (2.24)$$

Rearranging shows

$$A_p = A_c \cdot W_a = \frac{\max\{V_i, V_o\} \cdot I_{Lrms}}{K_u \cdot B_{\max} \cdot f_{sw} \cdot J_m} \dots (2.25)$$

where A_p is the area product of the transformer. And thus the apparent power P_t is

$$P_t = \max\{V_i, V_o\} \cdot I_{Lrms} \dots (2.26)$$

2.4 Drawbacks of DAB with Phase-shift Modulation

From the analysis in Section 2.2.2, there is a minimum power requirement for soft-switching operation when d is not equal to one. In another word, when the transferred power is less than this minimum power requirement, either the leading bridge or the lagging bridge would experience hard switching depends on d is greater or less than one. Thus the converter efficiency is reduced at light load. Hence clearly DAB with PSM control only has a limited ZVS region for both input and output bridges. In addition, the high circulating current at light load, as analyzed in reference [11], is also a major problem of DAB that impacts the conversion efficiency of DAB converter.

2.5 Summary

In this chapter, the basic analysis of DAB converter is presented. The high frequency transformer design issues are presented as well. Based on the analysis, some drawbacks of DAB converter are inevitable with traditional PSM control. To overcome the limited ZVS range problem, a PWM control of DAB is introduced and analyzed in Chapter 3.

Chapter 3. Analysis of Dual Active Bridge with PWM Control

3.1 Introduction

Although DAB converter with phase-shift control has many advantages, it also has two main drawbacks: 1) limited ZVS range at light load; 2) high circulating energy/current at light load. And these drawbacks get even worse for some applications requiring wide input/output voltage variations or power variations; for example, in three-stage SST, the load of DAB is a PWM inverter followed by a load with an instantaneous power from zero to twice inverter average output power. Thus for these kinds of applications, a new modulation method should be applied to DAB converter to overcome above drawbacks. There are many published approaches addressing this problem, such as [12], [13] and so on. Among them, the PWM control of DAB [14] is selected to be studied and eventually applied to the DAB converter in the SST. Unlike traditional PSM control that only adjust the phase-shift between input bridge and output bridge of DAB to control the power transferred, the PWM control, furthermore, can adjust the phase-shift between two legs within either input or output bridge at one time or both bridges simultaneously as well. In this Chapter below, a comprehensive analysis of PWM control of DAB is presented.

3.2 Single PWM Control of DAB

3.2.1 Buck Mode

Fig. 3.1 shows the operation (within ZVS range) waveforms of DAB with single PWM control for buck mode ($d < 1$), where the output side (secondary side) voltage of transformer V_s is still a square wave with a duty cycle of 0.5 as with the PSM control while the transformer primary voltage V_p has a duty cycle less than 0.5. This is because there is a phase-shift α_p between two legs within input bridge (leading bridge), which means a freewheeling interval when the transformer leakage inductance current goes through the upper or the lower both two switches in the input bridge. It is clearly shown in Fig. 3.1 that the second half cycle waveform of leakage inductance current is symmetrical with that of the first half cycle regarding to the horizontal axis. Only first half cycle is therefore analyzed hereinafter.

3.2.1.1 Operation Principles and Soft-Switching Constraints

From the method in Section 2.2.1, the expressions of $i_L(0)$, $i_L(\alpha_p)$ and $i_L(\alpha_p + \phi)$ for buck mode are derived and shown as below,

$$i_L(0) = -\frac{V_i}{\omega L} [d\phi + (d - \frac{1}{2})\alpha_p + \pi(\frac{1-d}{2})] \quad \dots (3.1)$$

$$i_L(\alpha_p) = -\frac{V_i}{\omega L} [d\phi - \frac{\alpha_p}{2} + \pi(\frac{1-d}{2})] \quad \dots (3.2)$$

$$i(\alpha_p + \phi) = \frac{V_i}{\omega L} \left[\phi + \frac{\alpha_p}{2} - \pi \left(\frac{1-d}{2} \right) \right] \quad \dots (3.3)$$

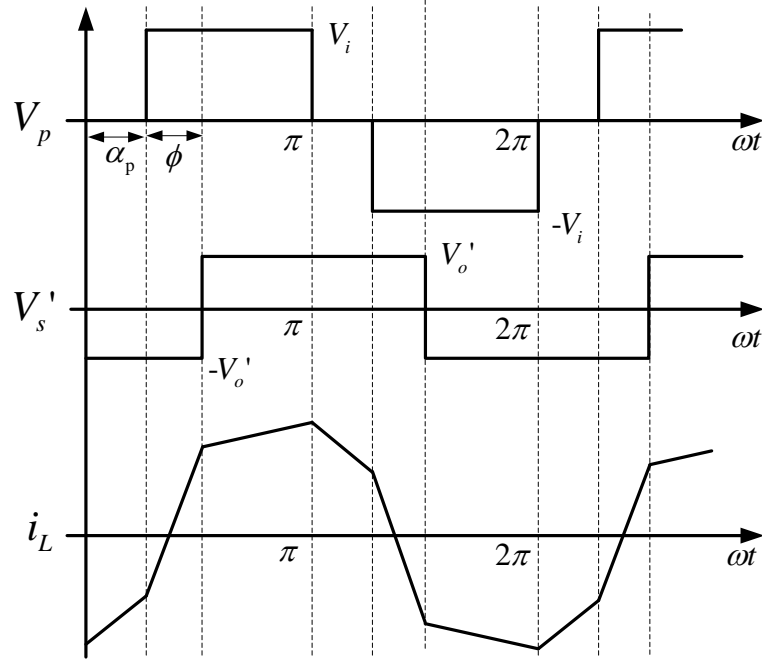


Fig. 3.1 Operation Waveforms within ZVS Range with Single PWM Control for
Buck Mode

Then the output power is derived as

$$P_o = \frac{V_i^2}{\omega L} d \cdot \left[\phi_f \left(1 - \frac{\phi_f}{\pi} \right) - \frac{\alpha_p^2}{4\pi} \right] \quad \dots (3.4)$$

where ϕ_f is the phase-shift between the fundamental components of V_p and V_s' , defined as

$$\phi_f = \phi + \alpha_p/2 \quad \dots (3.5)$$

The amount of output power is now controlled by ϕ_f instead of ϕ . During the forward power flow, ϕ_f is positive as similar with PSM control in which ϕ is positive. When reverse power flow ϕ_f is negative.

The constraints to achieve soft-switching for leading and lagging leg of input and output bridges can now be specified as

$$i_L(0) < 0 \quad \dots (3.6)$$

$$i_L(\alpha_p) < 0 \quad \dots (3.7)$$

$$i_L(\alpha_p + \phi) > 0 \quad \dots (3.8)$$

To get the minimum output power within ZVS range, from the observation of eqn. (3.4), ϕ_f should be minimized and oppositely α_p is supposed to be maximized. According to eqn. (3.1) and eqn. (3.6), when $0.5 < d < 1$, increase of α_p will extend the soft-switching range of the leading leg of input bridge while, according to eqn. (3.2), this increment will decrease the absolute value of $i_L(\alpha_p)$ until it reaches zero which violates the soft-switching requirement shown in eqn. (3.7) and consequently the lagging leg of the input bridge will experience hard switching. Thus the maximum/optimal α_p is found by setting $i_L(\alpha_p)$ equals to zero,

$$\alpha_p = 2d\phi + \pi(1-d) \quad \dots (3.9)$$

Substitute eqn. (3.9) into eqn. (3.5),

$$\phi_f = \pi(1-d)/2 + (1+d)\phi \quad \dots (3.10)$$

It should be noted that, from eqn. (3.9) and eqn. (3.10), maximizing α_p and minimizing ϕ_f are conflicted because they both positively related to ϕ . Through the numerical verification, it is found that the output power depends more on ϕ_f than on α_p . Therefore, by setting ϕ equals to zero, the optimal α_p and corresponding ϕ_f values are derived as

$$\alpha_{p,opt} = \pi(1-d) \quad \dots (3.11)$$

$$\phi_{f,min} = \pi \cdot (1-d)/2 \quad \dots (3.12)$$

Consequently the output power with soft-switching operation is lowest, which means the ZVS range is maximized. Substitute eqn. (3.11) and eqn. (3.12) into eqn. (3.4), the minimum output power with soft-switching operation is

$$P_{o,min,singlePWM} = \frac{V_i^2}{\omega L} \cdot \frac{\pi}{2} (1-d) \cdot d^2 \quad \dots (3.13)$$

The minimum power within ZVS range with traditional PSM and with single PWM control is plotted in Fig. 3.2 for comparison. It is shown that as d decreases, the single PWM control can reduce the minimum power within ZVS range by 10% of the rated power at most. During the operation, if α_p value is fixed as $\alpha_{p,opt}$ the transferred power operated within ZVS is lowest; for further lower power operation (waveforms shown in Fig. 3.3) with single PWM control, ϕ needs to be negative which consequently causes hard switching in output

bridge (both legs) of DAB. A dual PWM control is, therefore, introduced to extend ZVS range down to zero load in Section 3.3.

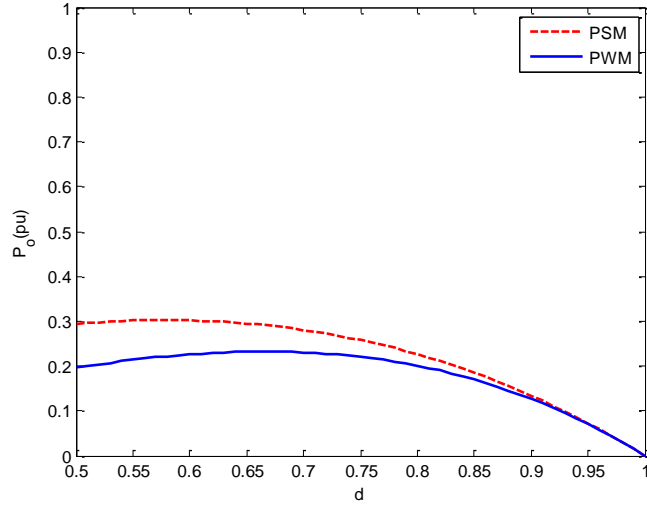


Fig. 3.2 Minimum Power within ZVS Range with PSM and Single PWM Control

for Buck Mode

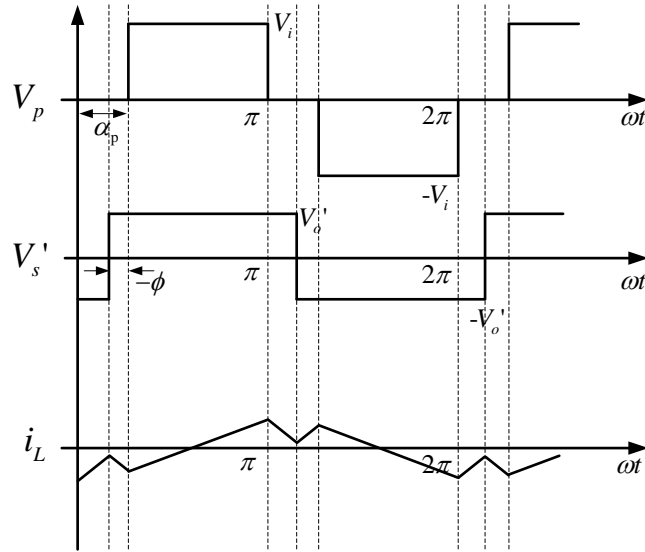


Fig. 3.3 Operation Waveforms Out of ZVS Range with Single PWM Control for

Buck Mode

3.2.2 Boost Mode

For boost mode operation, opposite as buck mode, transformer primary side voltage V_p is a square wave with a duty cycle of 0.5 while in the output bridge a phase-shift α_s is introduced between two legs. The operation (within ZVS range) waveforms are shown in Fig. 3.4

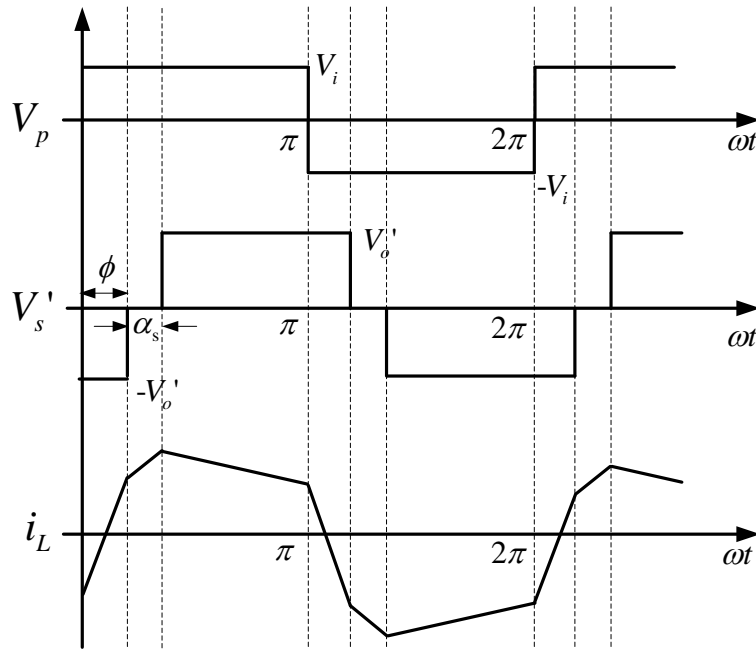


Fig. 3.4 Operation Waveforms within ZVS Range with Single PWM Control for
Boost Mode

Similar as the analysis in Section 3.2.1, the output power for boost mode is derived as

$$P_o = \frac{V_i^2}{\omega L} d \cdot \left[\phi_f \left(1 - \frac{\phi_f}{\pi} \right) - \frac{\alpha_s^2}{4\pi} \right] \quad \dots (3.14)$$

where ϕ_f , defined as $\phi + \alpha_s/2$, is the phase-shift between fundamental components of V_p and V_s' . To get the minimum transferred power within ZVS range, optimal α_s and corresponding $\phi_{f,\min}$ are found as

$$\alpha_{s,opt} = \pi(1-1/d) \dots (3.15)$$

$$\phi_{f,\min} = \pi \cdot (1-1/d)/2 \dots (3.16)$$

Substitute eqn. (3.15) and eqn. (3.16) into eqn. (3.14), the minimum power within ZVS range is

$$P_{o,\min,\text{singlePWM}} = \frac{V_i^2}{\omega L} \cdot \frac{\pi}{2} (d-1) / d^2 \dots (3.17)$$

Fig. 3.5 shows the minimum power with soft-switching operation with PSM and single PWM controls. It is clearly that for boost mode, the ZVS range of DAB with single PWM control is much larger than that of DAB with traditional PSM control. It is shown that, when d is greater than 1.82, the input bridge will experience the hard switching for even the rated power. For further lower power operation (waveforms shown in Fig. 3.6) with single PWM control, ϕ needs to be negative and consequently cause hard switching in input bridge (both legs) of DAB converter.

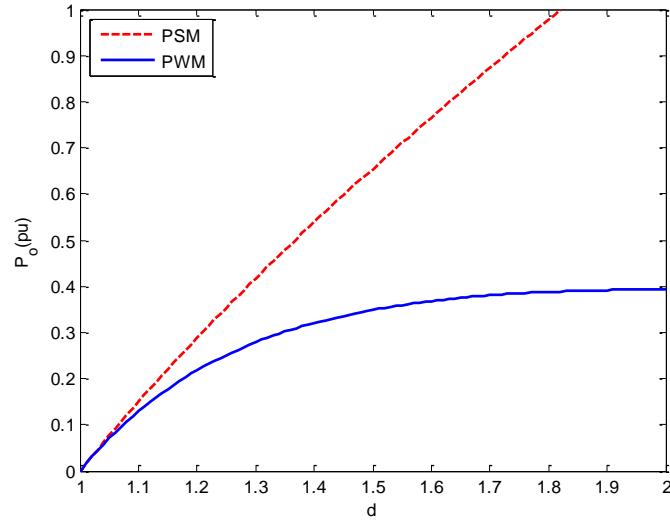


Fig. 3.5 Minimum Power within ZVS Range with PSM and Single PWM Control

for Boost Mode

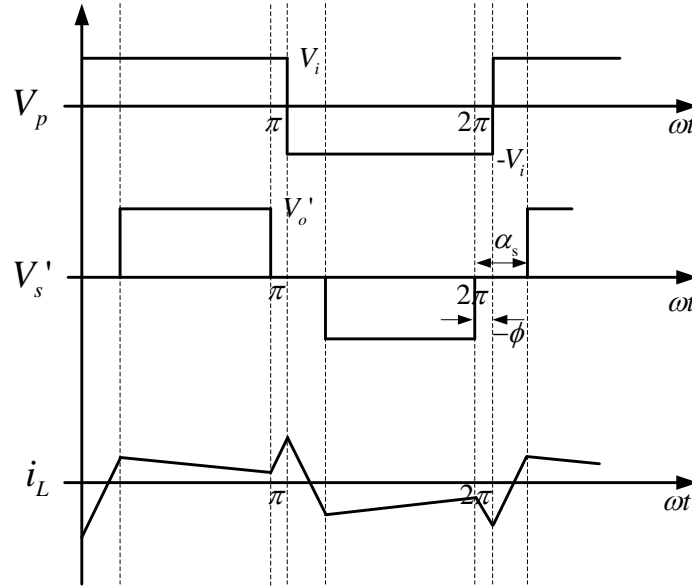


Fig. 3.6 Operation Waveforms Out of ZVS Range with Single PWM Control for

Boost Mode

3.2.3 Transformer Design for DAB with Single PWM

Buck Mode

From Fig. 3.1, the volt-second applied to transformer is

$$\text{volt-second} = (V_i + V_o) \cdot \frac{\phi}{2\pi} \cdot T_s + (V_i - V_o) \cdot \frac{\pi - \phi - \alpha_p}{2\pi} \cdot T_s \quad \dots (3.18)$$

Combined with eqn. (3.11),

$$\text{volt-second} = \frac{(1-d)V_i \cdot \pi \cdot d + 2d \cdot V_i \cdot \phi}{2\pi} \cdot T_s \quad \dots (3.19)$$

The maximum volt-second occurs at

$$\phi = \phi_{\max} = \phi_{f\max} - \frac{\alpha_p}{2} = \frac{\pi d}{2} \quad \dots (3.20)$$

Thus the maximum volt-second is

$$\text{volt-second}_{\max} = \frac{V_i d}{2} \cdot T_s \quad \dots (3.21)$$

Boost Mode

From Fig. 3.4, when boost mode, the volt-second is

$$\text{volt-second} = (V_i + V_o) \cdot \frac{\phi}{2\pi} \cdot T_s + V_i \cdot \frac{\alpha_s}{2\pi} \cdot T_s \quad \dots (3.22)$$

when $\phi = \phi_{\max} = \phi_{f\max} - \frac{\alpha_s}{2} = \frac{\pi}{2d}$, with eqn. (3.15),

$$\text{volt-second}_{\max} = \frac{(3d-1)V_i}{4d} \cdot T_s \quad \dots (3.23)$$

Using the same method in Section 2.3, the apparent power of the transformer for both buck and boost modes could be derived as

$$P_t = V_i d \cdot I_{Lrms} \quad (d < 1) \quad \dots \quad (3.24)$$

$$P_t = \frac{(3d-1)V_i}{2d} \cdot I_{Lrms} \quad (d > 1) \quad \dots \quad (3.25)$$

and it can be proved that the maximum apparent power occurs at maximum d situation. As d changes, when maximum power ($\phi = \pi/2$ or $\phi_f = \pi/2$), the apparent power with PSM and single PWM control is plotted in Fig. 3.7. It is shown that, no matter in buck or boost mode, the transformer apparent power with single PWM Control is less than the apparent power with PSM control and therefore the size/weight of the high frequency transformer is reduced. Also, the transformer apparent power with single PWM control is plotted in Fig. 3.8 while d and ϕ_f are changing.

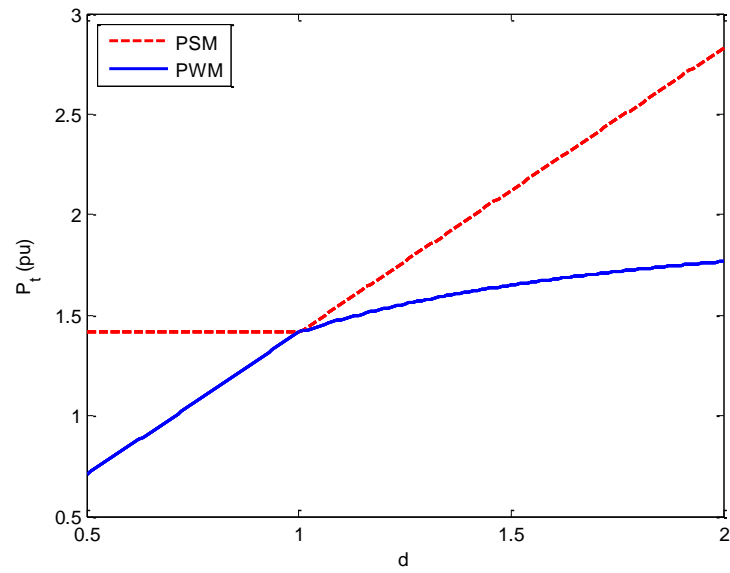


Fig. 3.7 Transformer Apparent Power When Maximum Output Power with PSM
and Single PWM Control

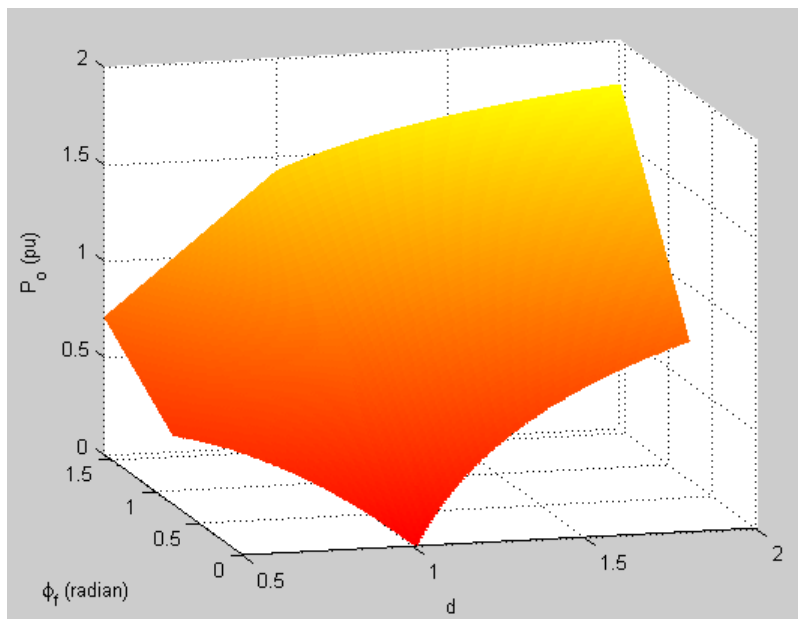


Fig. 3.8 Transformer Apparent Power with Single PWM Control

3.3 Dual PWM Control of DAB

As discussed above, the single PWM control of DAB is not able to reduce ZVS range down to zero load; thus, a simultaneously dual PWM control is introduced by other scholars to achieve zero load with soft-switching. Fig. 3.9 shows the operation waveforms of DAB with dual PWM control for buck mode. In this Chapter, only buck mode is analyzed due to the duality between buck mode and boost mode. In dual PWM control, both primary and secondary side voltages V_p and V_s have a duty cycle less than 0.5 caused by two simultaneously phase-shifts α_p and α_s between two legs within both bridges.

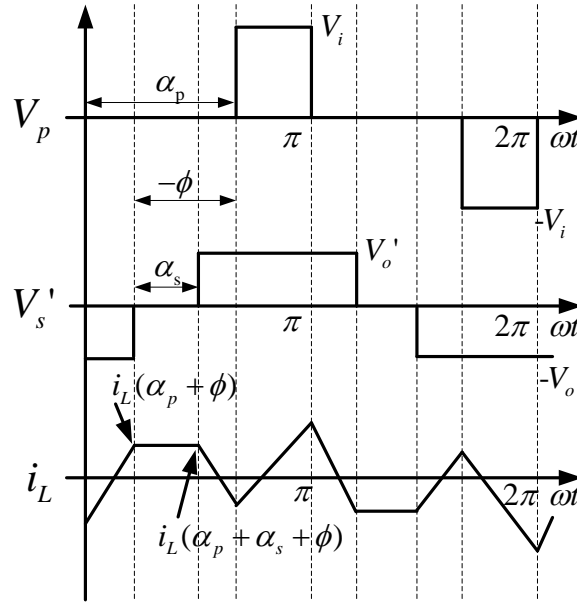


Fig. 3.9 Operation Waveforms of DAB with Dual PWM Control for Buck Mode

From the same method in Section 2.2.1, the expressions of $i_L(0)$, $i_L(\alpha_p + \phi)$, $i_L(\alpha_p + \alpha_s + \phi)$ and $i_L(\alpha_p)$ are shown below,

$$i_L(0) = -\frac{V_i}{\omega L} \left(\frac{1-d}{2} \cdot \pi + d\phi_f + \frac{d-1}{2} \cdot \alpha_p \right) \quad \dots (3.26)$$

$$i_L(\alpha_p + \phi) = \frac{V_i}{\omega L} \left(\frac{d-1}{2} + \frac{\alpha_p}{2} - \frac{d \cdot \alpha_s}{2} \right) \quad \dots (3.27)$$

$$i_L(\alpha_p + \alpha_s + \phi) = \frac{V_i}{\omega L} \left(\frac{d-1}{2} + \frac{\alpha_p}{2} - \frac{d \cdot \alpha_s}{2} \right) \quad \dots (3.28)$$

$$i_L(\alpha_p) = -\frac{V_i}{\omega L} \left(\frac{1-d}{2} \cdot \pi - d\phi_f + \frac{d-1}{2} \cdot \alpha_p \right) \quad \dots (3.29)$$

Then the output power is derived as

$$P_o = \frac{V_i^2}{\omega L} d \cdot \phi_f \left(1 - \frac{\alpha_p}{\pi} \right) \quad \dots (3.30)$$

where ϕ_f is the phase-shift between fundamental components of V_p and V_s' , defined as

$$\phi_f = \phi + \alpha_s/2 + \alpha_p/2 \quad \dots (3.31)$$

To achieve soft-switching for all switches of DAB, it is implied that

$$i_L(0) < 0 \quad \dots (3.32)$$

$$i_L(\alpha_p + \phi) > 0 \quad \dots (3.33)$$

$$i_L(\alpha_p + \alpha_s + \phi) > 0 \quad \dots (3.34)$$

$$i_L(\alpha_p) < 0 \quad \dots (3.35)$$

To find the optimal α_p and α_s values for soft-switching, the circulating energy analysis is necessarily presented below. Fig. 3.10 repeats the operation

waveforms to better illustrate circulating energy. In the third plot, the darker shaded area shows the circulating energy between input port and transformer leakage inductance while the lighter area presents the freewheeling current/energy in the primary winding; In the bottom plot, the darker and lighter shaded areas indicate the circulating energy between output port and leakage inductance and the freewheeling energy in the secondary winding respectively. In both plots, the unshaded area shows the energy/power transferred from input to output. It is obvious that the output power is only dependent on the absolute value of $i_L(0)$; the rms current is related to $i_L(\alpha_p + \phi)$, $i_L(\alpha_p + \alpha_s + \phi)$ and $i_L(\alpha_p)$ besides $i_L(0)$. Thus $i_L(\alpha_p + \phi)$, $i_L(\alpha_p + \alpha_s + \phi)$ and $i_L(\alpha_p)$ should be minimized to reduce transformer leakage inductance rms current meanwhile satisfying the ZVS conditions. Then theoretically α_p and α_s are found by setting

$$i_L(\alpha_p + \phi) = i_L(\alpha_p + \alpha_s + \phi) = i_L(\alpha_p) = 0 \quad \dots (3.36)$$

Thus,

$$\alpha_{p,opt} = \pi - \frac{2d\phi_f}{1-d} \quad \dots (3.37)$$

$$\alpha_{s,opt} = \pi - \frac{2\phi_f}{1-d} \quad \dots (3.38)$$

From eqn. (3.31), eqn. (3.37) and eqn. (3.38), ϕ_f can down to zero with a ϕ of $-\pi$, which is possible for dual PWM control. Then the corresponding $\alpha_p = \pi$ and $\alpha_s = \pi$ ensure the ZVS range down to zero power. Therefore with

dual PWM Control, all 8 devices can achieve soft-switching and the minimum power transferred can be reduced to zero.

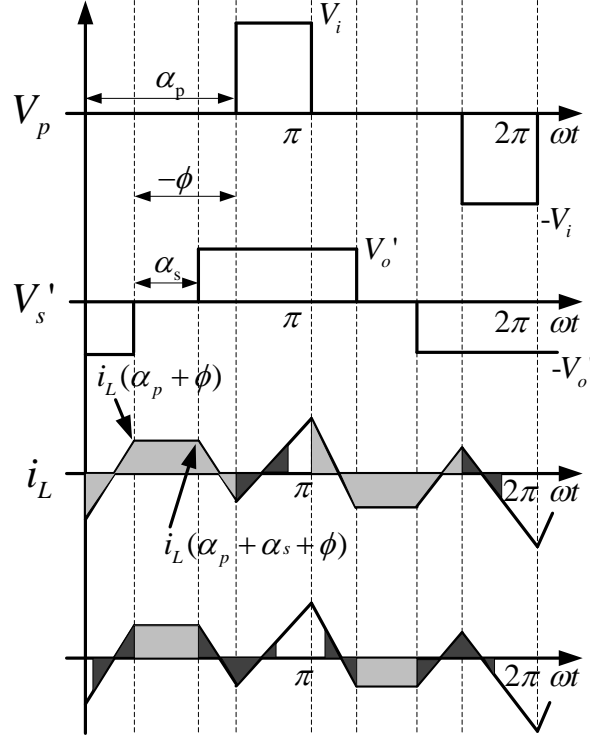


Fig. 3.10 Operation Waveforms Illustrating Circulating Energy

3.4 Composite Scheme

From the analysis of dual PWM control above, as power increases, ϕ_f increases till ϕ_f equals to $\pi(1-d)/2$, which causes α_s equals to zero and α_p is decreased to $\pi(1-d)$, the optimal α_p value for single PWM control. Then the modulation transfers from dual PWM control to single PWM control seamlessly. With a specified d equals to 0.5, the value of α_p and α_s as power increases is shown in Fig. 3.11. It has been seen that, with PSM control the

converter will experience hard switching at light load while can achieve ZVS down to zero load with PWM control. However, Fig. 3.11 also shows that the maximum power capability by PWM control is less than the capability obtained by traditional PSM control; and this is one major drawback of single PWM control. Furthermore, considering the variation of d , Fig. 3.12 is plotted showing that as d is closing to one, the loss of power capability is decreasing. However, when d is smaller, the ZVS range advantage of PWM control is more obvious over PSM.

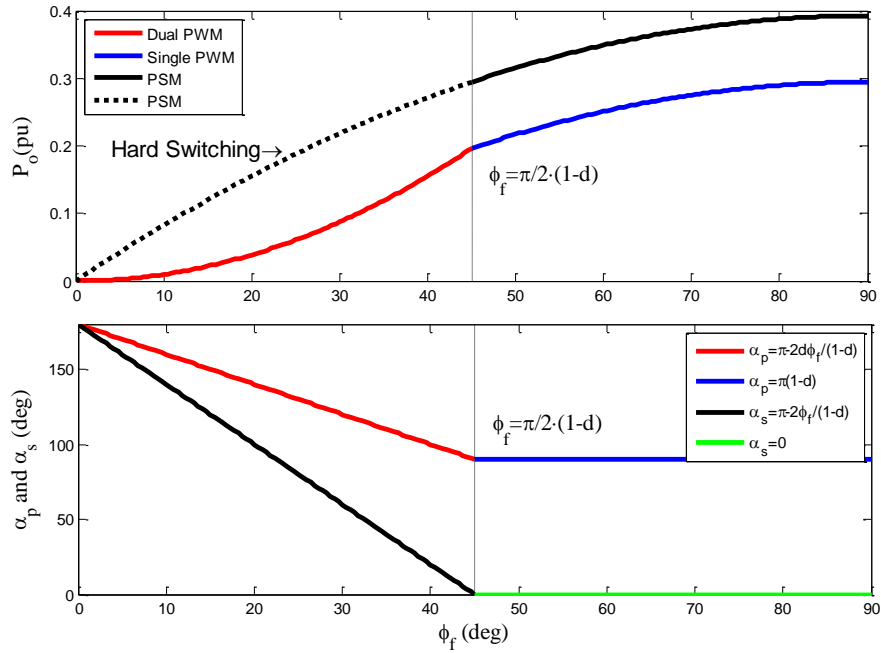


Fig. 3.11 DAB Output Power versus ϕ_f with a specified d

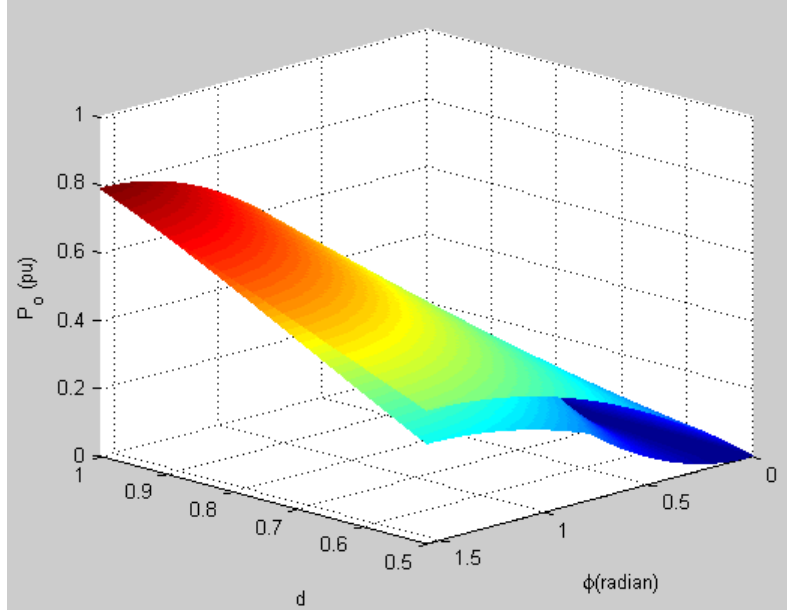


Fig. 3.12 DAB Output Power versus ϕ_f and d with PSM and PWM Control

3.5 Effect of Switch Output Capacitance

From previous analysis, the optimal α_p is found by setting $i_L(\alpha_p)$ equals to zero for single PWM control and the optimal α_p and α_s for dual PWM control are found by setting $i_L(\alpha_p + \phi)$, $i_L(\alpha_p + \alpha_s + \phi)$ and $i_L(\alpha_p)$ to be zero; however for practical converter, at these transition points, the leakage inductance current/energy should be large enough to charge and discharge devices' output capacitance and deliver energy to either input or output port. Therefore, there should be some modifications of the optimal α_p and α_s values and minimum requirement of ϕ for both single PWM control and dual PWM control. Assume that

$$\phi = \phi_{\min} > 0 \quad \dots (3.39)$$

$$\alpha_p = \alpha_{p,opt} - \Delta_p \quad \dots (3.40)$$

$$\alpha_s = \alpha_{s,opt} - \Delta_s \quad \dots (3.41)$$

3.5.1 Analysis for Single PWM Situation

Fig. 3.13 repeats the operation waveforms of DAB with single PWM control for buck mode, in which the minimum current requirements for the turn-on transition of the lagging leg of the input bridge and the leading leg of the output bridge are shown. The turn-on transition procedure of the lagging leg of the input bridge is shown in Fig. 3.14 and the turn-on transition of the leading leg of output bridge refers to Fig. 2.4(b)-(e). It is assumed that the output capacitance of all eight switches in both input and output bridges is the same, presented by C_s .

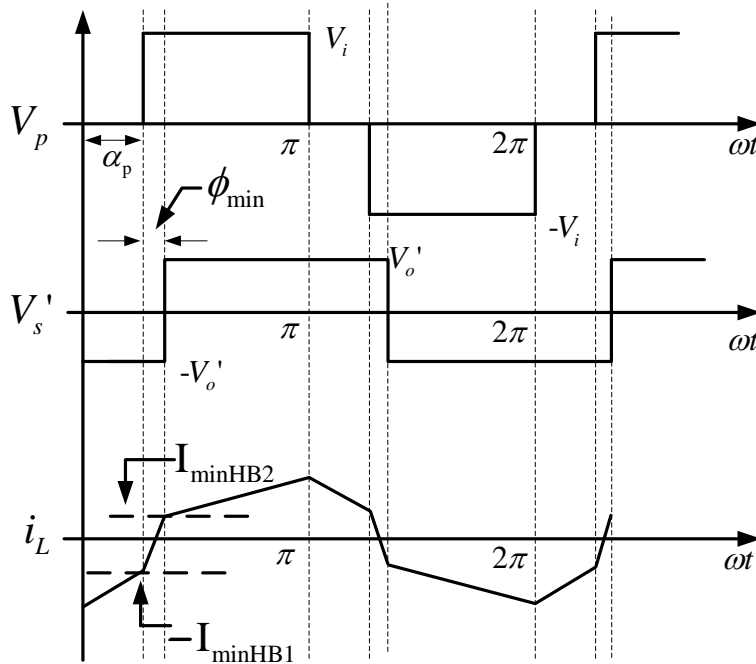


Fig. 3.13 Operation Waveforms of DAB with Single PWM Control

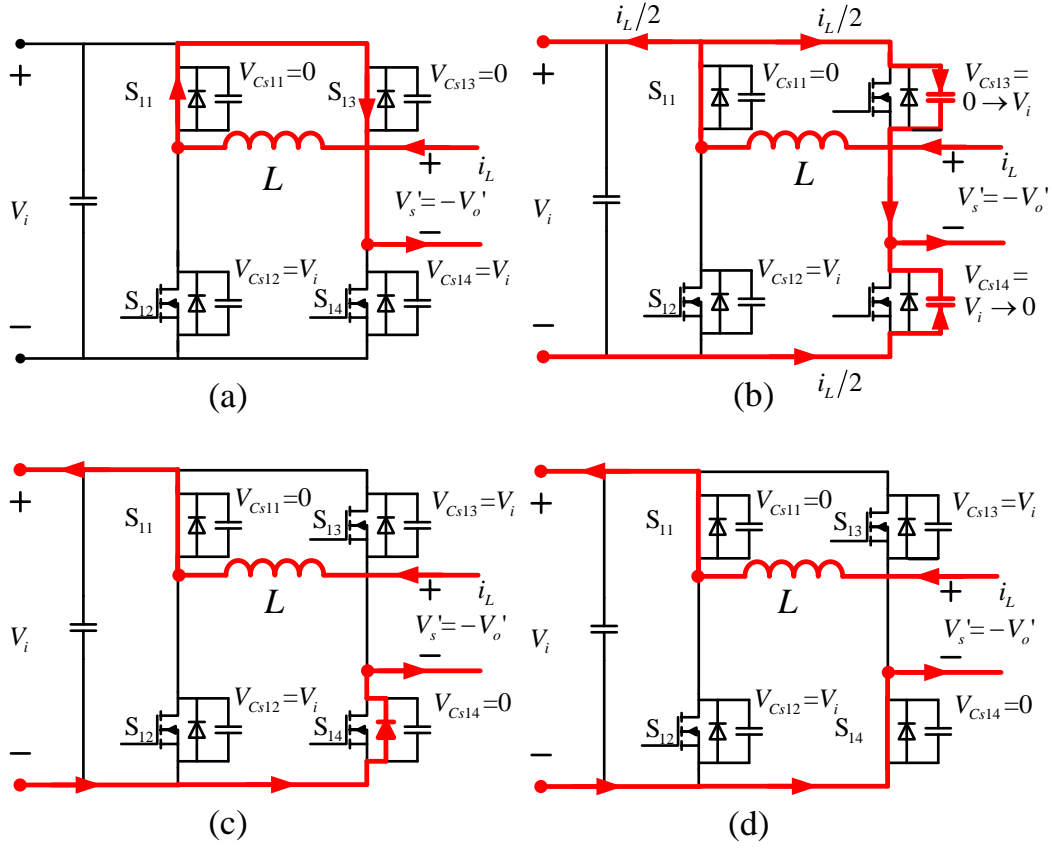


Fig. 3.14 Transition Procedure of Switch S_{14} in the Input Bridge

Before the turn-on transition of switch S_{14} , as shown in Fig. 3.14(a), the upper two switches of the input bridge are freewheeling. The transition starts by the turn-off of S_{13} and then the leakage inductance current separates to two equal parts to discharge C_{s14} through input voltage V_i and charge C_{s13} in a resonant manner till the voltage across C_{s14} gets zero while the voltage across C_{s13} reaches V_i . Then if the current is still negative, the body diode of S_{14} , D_{14} , will turn on clamping the voltage across S_{14} to zero (assuming zero on-state drop voltage of D_{14}) and thus achieve zero-voltage turn-on of switch S_{14} .

Let us assume at $t=t_0$ transition starts and at $t=t_m$ the transition finishes and after the transition, the transformer leakage inductance current i_L just reaches zero. Thus at $t=t_0$,

$$i_L = i_L(\alpha_p) = -I_{\min HB1}$$

$$V_{C_{s13}} = 0$$

$$V_{C_{s14}} = V_i$$

and at $t=t_m$,

$$i_L = i_L(\alpha_p) = 0$$

$$V_{C_{s13}} = V_i$$

$$V_{C_{s14}} = 0$$

In the transition,

$$\frac{i_L}{2} = C_s \frac{dv}{dt} = \frac{C_s \cdot V_i}{dt} \quad \dots (3.42)$$

Since $C_{s13} = C_{s14} = C_s$, the energy in c at $t=t_0$ is the same as the energy in C_{s13} at $t=t_m$. Then consider the energy balance (ignoring the loss in the circuit),

$$\frac{1}{2} L I_{\min HB1}^2 + \int_{t_0}^{t_m} (-V_o') i_L dt = \int_{t_0}^{t_m} V_i \cdot \frac{i_L}{2} dt \quad \dots (3.43)$$

Combined with eqn. (3.41),

$$I_{\min HB1} = \sqrt{\frac{2C_s V_i^2 \cdot (1+2d)}{L}} = \frac{\sqrt{2V_i^2 \cdot (1+2d)}}{Z_0} \quad \dots (3.44)$$

where $Z_0 = \sqrt{\frac{L}{C_s}}$. And thus,

$$i_L(\alpha_p) = -\frac{V_i}{\omega L} \left[d\phi - \frac{\alpha_p}{2} + \pi \left(\frac{1-d}{2} \right) \right] = -I_{\min \text{HB1}} \quad \dots (3.45)$$

Substitute eqn. (3.39) and eqn. (3.40) into above equation,

$$\frac{V_i}{\omega L} \left(d\phi_{\min} + \frac{\Delta_p}{2} \right) = I_{\min \text{HB1}} \quad \dots (3.46)$$

For the output bridge transition, S_{22} and S_{23} are turned off simultaneously and the leakage inductance current separates to two equal parts to discharge C_{s21} , C_{s24} and charge C_{s22} , C_{s23} directly (without going through output port). Thus there is no energy consumed by the output at this transition. Ignoring circuit loss,

$$\frac{1}{2} L I_{\min \text{HB2}}^2 + \int_{t_0}^{t_m} V_i i_L dt = 0 \quad \dots (3.47)$$

Eqn. (3.45) could be solved that

$$i_L = i_L(\alpha_p + \phi) = I_{\min \text{HB2}} = 0 \quad \dots (3.48)$$

Combined with eqn. (3.3), eqn. (3.39) and eqn. (3.40),

$$i_L(\alpha_p + \phi) = \frac{V_i}{\omega L} \left(\phi_{\min} - \frac{\Delta_p}{2} \right) = I_{\min \text{HB2}} = 0 \quad \dots (3.49)$$

Therefore, from eqn. (3.44), eqn. (3.46) and eqn. (3.49),

$$\phi_{\min} = \frac{\sqrt{2(1+2d)}}{1+d} \cdot \frac{\omega}{\omega_r} \quad \dots (3.50)$$

where $\omega_r = 1/\sqrt{LC_s}$. And

$$\Delta_p = 2\phi_{\min} = \frac{2\sqrt{2(1+2d)}}{1+d} \cdot \frac{\omega}{\omega_r} \quad \dots (3.51)$$

For boost mode, a similar analysis shows that

$$\phi_{\min} = \frac{2\sqrt{d}}{1+d} \cdot \frac{\omega}{\omega_r} \quad \dots (3.52)$$

$$\Delta_s = \frac{2\phi_{\min}}{d} = \frac{4}{\sqrt{d}(1+d)} \cdot \frac{\omega}{\omega_r} \quad \dots (3.53)$$

3.5.2 Analysis for Dual PWM Situation

Fig. 3.15 repeats the operation waveforms of DAB with dual PWM control for buck mode, in which the minimum current requirements for the turn-on transition of the lagging leg of both input and output bridges are shown. Fig. 3.16 shows the turn-on transition procedure of the lagging leg in the output bridge while Fig. 3.17 indicates the turn-on transition of the lagging leg in the input bridge.

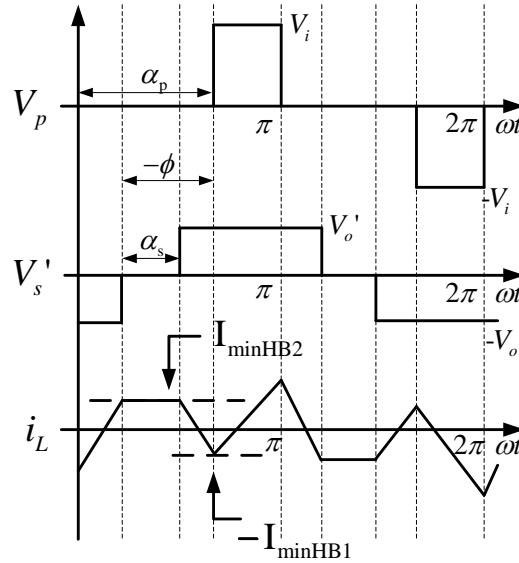


Fig. 3.15 Operation Waveforms of DAB with Dual PWM Control

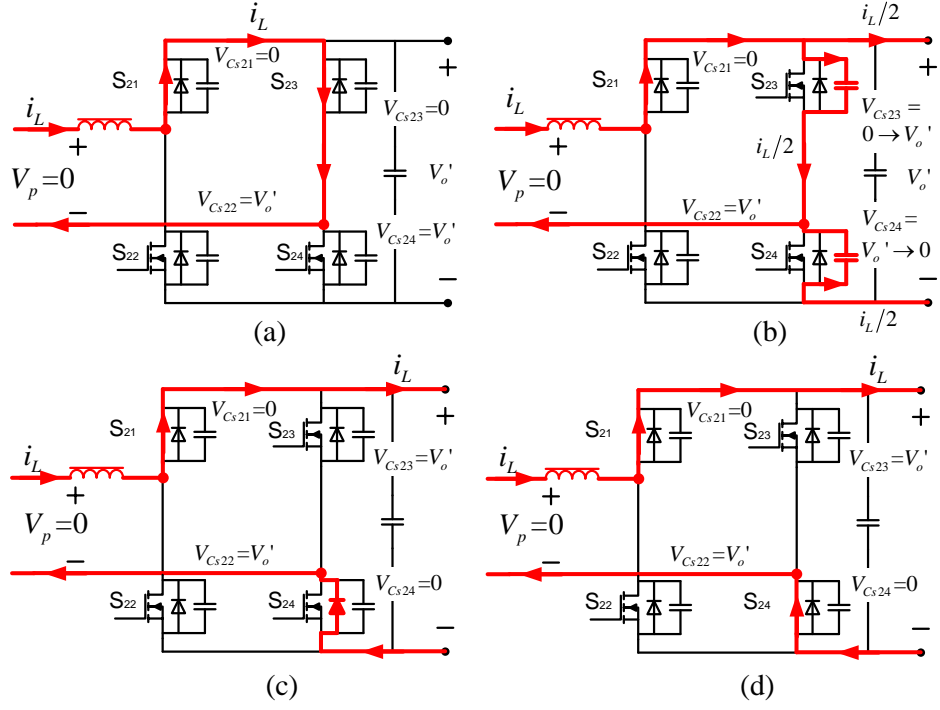


Fig. 3.16 Turn-on Transition Procedure of the Lagging Leg in the Output Bridge

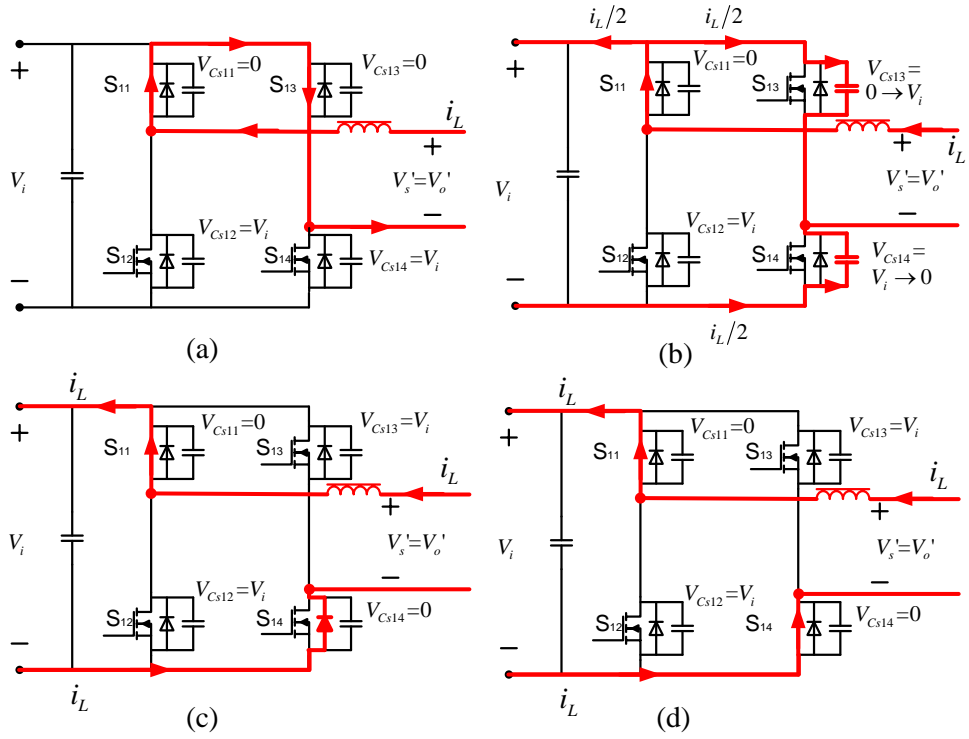


Fig. 3.17 Turn-on Transition of the Lagging Leg in the Input Bridge

It is shown in Fig. 3.16 that, to achieve the zero-voltage switching of the output bridge, the initial leakage inductance current should be large enough to match the energy transferred to output port during the transition. Thus,

$$\frac{1}{2} L I_{\min HB2}^2 = \int_{t_0}^{t_m} \frac{i_L}{2} \cdot V_o' dt \quad \dots (3.54)$$

And during the transition,

$$\frac{i_L}{2} = C_s \frac{dv}{dt} = C_s \frac{V_o'}{dt} \quad \dots (3.55)$$

From eqn. (3.54) and eqn. (3.55),

$$I_{\min HB2} = \frac{\sqrt{2d} \cdot V_i}{Z_o} \quad \dots (3.56)$$

where $Z_o = \sqrt{\frac{L}{C_s}}$. And thus,

$$i_L(\alpha_p + \alpha_s + \phi) = \frac{V_i}{\omega L} \left(\frac{d-1}{2} + \frac{\alpha_p}{2} - \frac{d \cdot \alpha_s}{2} \right) = I_{\min HB2} \quad \dots (3.57)$$

Substitute eqn. (3.40) and eqn. (3.41) into eqn. (3.57),

$$\frac{V_i}{\omega L} \left(-\frac{1}{2} \Delta_p + \frac{d}{2} \Delta_s \right) = I_{\min HB2} \quad \dots (3.58)$$

For the input bridge to obtain zero-voltage switching as shown in Fig. 3.17, the initial energy stored in the leakage inductance plus the energy supplied from output port during the transition should match the energy consumed by the input port,

$$\frac{1}{2} L I_{\min HB1}^2 + \int_{t_0}^{t_m} i_L \cdot V_o' dt = \int_{t_0}^{t_m} \frac{i_L}{2} \cdot V_i dt \quad \dots (3.59)$$

During the transition,

$$\frac{i_L}{2} = C_s \frac{dv}{dt} = C_s \frac{V_i}{dt} \quad \dots (3.60)$$

Combined with eqn. (3.59) and eqn. (3.60),

$$I_{\min HB1} = \begin{cases} \frac{\sqrt{2(1-2d)} \cdot V_i}{Z_o} & (d < 0.5) \\ 0 & (0.5 < d < 1) \end{cases} \quad \dots (3.61)$$

And therefore,

$$i_L(\alpha_p) = -\frac{V_i}{\omega L} \left(\frac{1-d}{2} \cdot \pi - d\phi_f + \frac{d-1}{2} \cdot \alpha_p \right) = -I_{\min HB1} \quad \dots (3.62)$$

Combined with eqn. (3.40) and eqn. (3.41),

$$-\frac{V_i}{\omega L} \left(\frac{1-d}{2} \Delta_p \right) = -I_{\min HB1} \quad \dots (3.63)$$

Thus from eqn. (3.56), eqn. (3.58), eqn. (3.62) and eqn. (3.63),

$$\Delta_p = \begin{cases} \frac{2\sqrt{2(1-2d)}}{1-d} \cdot \frac{\omega}{\omega_r} & (d < 0.5) \\ 0 & (0.5 < d < 1) \end{cases} \quad \dots (3.64)$$

$$\Delta_s = \begin{cases} \left[2\sqrt{2} + \frac{2\sqrt{2(1-2d)}}{d(1-d)} \right] \cdot \frac{\omega}{\omega_r} & (d < 0.5) \\ 2\sqrt{2} \cdot \frac{\omega}{\omega_r} & (0.5 < d < 1) \end{cases} \quad \dots (3.65)$$

3.6 Summary

In this chapter, the PWM control of DAB converter is analyzed comprehensively and compared with the traditional PSM control demonstrating that, with PWM control, the ZVS rang of DAB can be extended to zero load and the circulating current at light load is minimized. In addition, for the high

frequency transformer, the apparent power and consequently the size of the transformer are reduced as well. Lastly the effect of the switch output capacitance is analyzed for practical implementation of the PWM control.

Chapter 4. PWM of DAB in the Solid-state Transformer

4.1 Introduction

For the DC/DC stage of SST, the dual active bridge converter (DAB) is preferred due to its simple structure, ZVS feature and seamless bi-directional power flow capability as mentioned in Chapter 2. However, DAB only has a limited ZVS range with traditional phase-shift (PSM) control when the ratio of referred output voltage to the input voltage differs from one, which leads to low efficiency at light load. In the SST, the load of dual active bridge is a PWM inverter that has an instantaneous load power varying from zero to twice the inverter rated power at twice the line frequency. In addition, the input of the SST is also an instantaneous power varies at the double line frequency, as shown in Fig. 4.1. One major challenge of DAB in SST is the size of intermediate DC link capacitors [15], including both high voltage and low voltage DC link capacitors. These large DC link capacitors are required to withstand the twice fundamental frequency power variation of the input and load of DAB. Then the DAB converter only process constant power, as shown in Fig. 4.2(a), for achieving high efficiency operation considering that the efficiency is low at light load with traditional PSM control as presented in Chapter 2. However, the large capacitors bring many problems, such as lower power density and reliability issues

associated with electrolytic capacitors. And even with large capacitors, when the average load is light, DAB with traditional PSM control still needs to process a low power and consequently operates with hard-switching, which is not desirable.

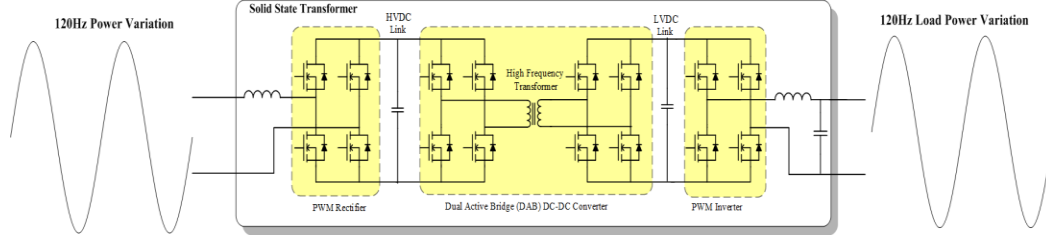


Fig. 4.1 DAB Converter in the SST

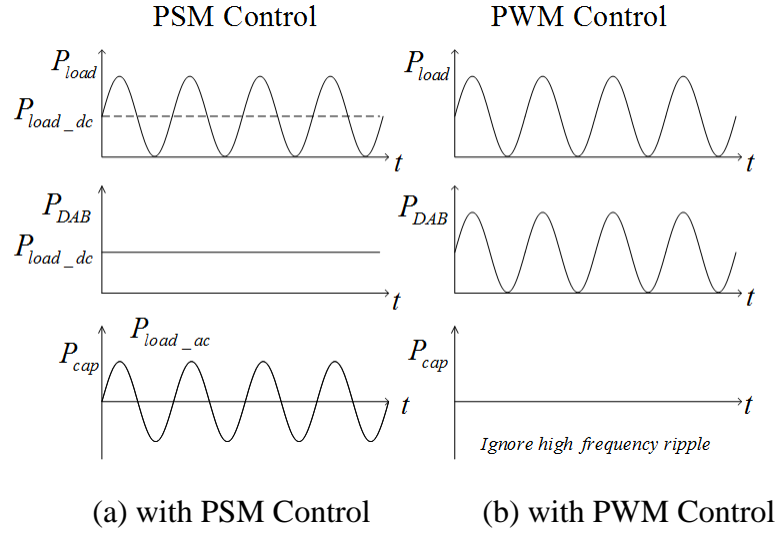


Fig. 4.2 Waveforms of Load Power, DAB Processing Power and Power Variation on DC link Capacitors

4.2 Converter Design and Capacitor Evaluation

4.2.1 Converter Design

Considering the available experiment conditions, a 40kHz, 500W DAB converter is designed for simulation and later experiment verification. The input

nominal voltage is 60V with a variation of 20% while the output voltage is 60V.

With design specifications, the turns ratio of high-frequency transformer is easily to be chosen as one. The total leakage inductance is, chosen at maximum power with an allowable maximum ϕ_f of 75° , 23.3 μ H . The design specifications are shown in Table 4-1.

Table 4.1 DAB Converter Specifications

Rated Power	500W
Input Voltage	48V-72V
Output Voltage	60V
Frequency	40kHz
Transformer Turns Ratio	1:1
Leakage Inductance	23.3 μ H

4.2.2 Capacitor Evaluation

In the SST application, the instantaneous load power of DAB is from zero to maximum power at the double line frequency. For the specific design in above section, the DC link capacitor is supposed to absorb or provide 250W when the load instantaneous power is 0W or 500W, as shown in Fig. 4.2(a). To maintain a peak-peak voltage ripple within 5V, capacitance is calculated as

$$C = \frac{I_{pk} \cdot 2}{\omega \cdot \Delta V} = \frac{250/60 \times 2}{2\pi \times 120 \times 5} = 2.21\text{mF}$$

where I_{pk} is the double-line frequency current ripple (peak current) at maximum power.

Usually the polypropylene film capacitor is preferred in the high power high frequency design due to its long lifetime and high performance in that it has very low dissipation factor, almost constant with temperature [16]. However, with such a large capacitance, film capacitor is really expensive which will increase the cost of converter considerably. And even much cheaper aluminum electrolytic capacitor with such a large capacitance and high voltage rating is very expensive for most designs. More importantly, the use of electrolytic capacitors will impact the performance of the converter. While with PWM control, DAB converter is theoretically able to handle all the power variation due to the inverter load. Ideally DC link capacitor has no need to withstand low frequency power variations, as shown in Fig. 4.2(b); the capacitor only needs to handle high frequency power ripple and thus can be much smaller, calculated as

$$C = \frac{I_{pk_sw} \cdot T_{sw} / 2}{\Delta V_{sw}} = \frac{12 \times 1 / (40000 \times 2)}{2.5} = 60 \mu F$$

where I_{pk_sw} is the switching frequency current ripple at maximum power and

ΔV_{sw} is high frequency voltage ripple requirement, which is 2.5V in this case.

However, as the 120Hz low frequency power processed by DAB is not exactly

matched with load instantaneous power in practical implementation, there is a low frequency voltage ripple at output as well.

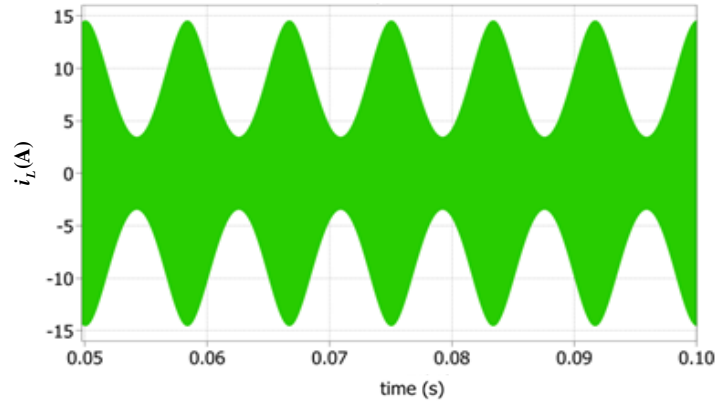
It has been seen that the DC link capacitors are reduced significantly from 2.21mF to 60 μ F, perfectly down to a value where electrolytic capacitors are not required. Thus the system performance, reliability and power density are ensured by using high performance, long lifetime and smaller film capacitors.

4.3 Simulation Results

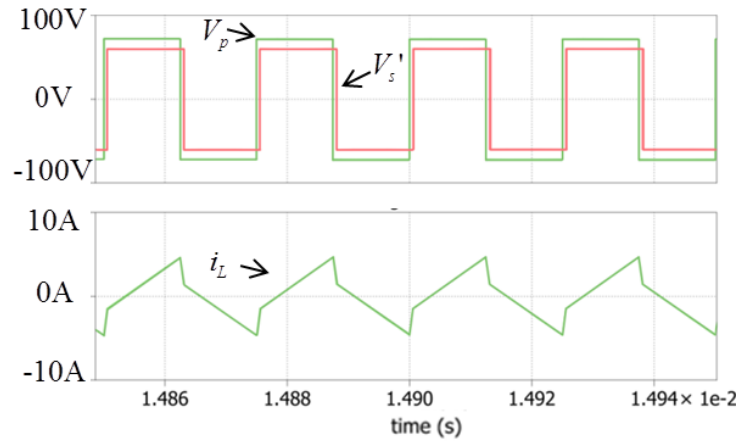
To verify the effect of PWM control of DAB converter in SST application, a simulation model of DAB with 500W rated power is built in PLECS software. The load of DAB, a PWM inverter, is simulated by a current source injecting the current with a double-line frequency. DAB converter operated with both PSM and PWM control is simulated to compare two modulation methods.

4.3.1 Simulation with PSM Control

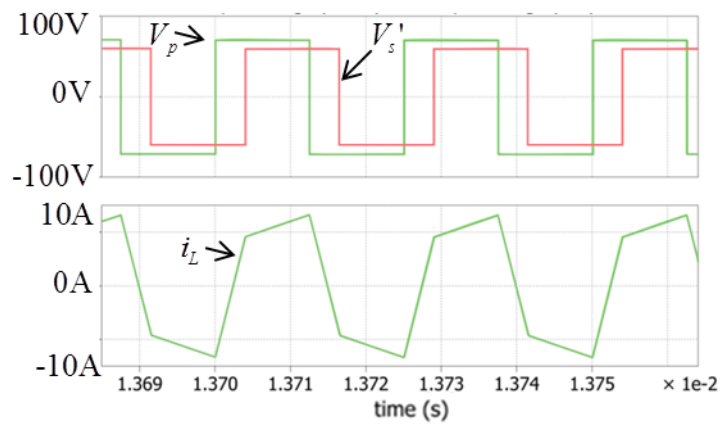
Fig. 4.3(a) shows the transformer leakage inductor current waveforms while Fig. 4.3(b) and 4.3(c) show the operation waveforms of DAB with PSM control at light load and maximum load respectively. The rms value of leakage inductance current is measured as 6.56A.



(a) Transformer Leakage Inductance Current under PSM Control



(b) Operation Waveforms of DAB with PSM Control at Light Load

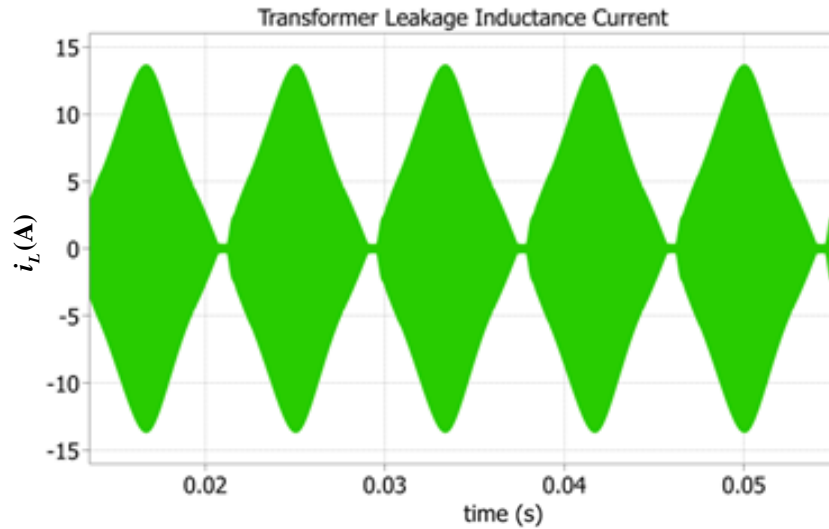


(c) Operation Waveforms of DAB with PSM Control at Heavy Load

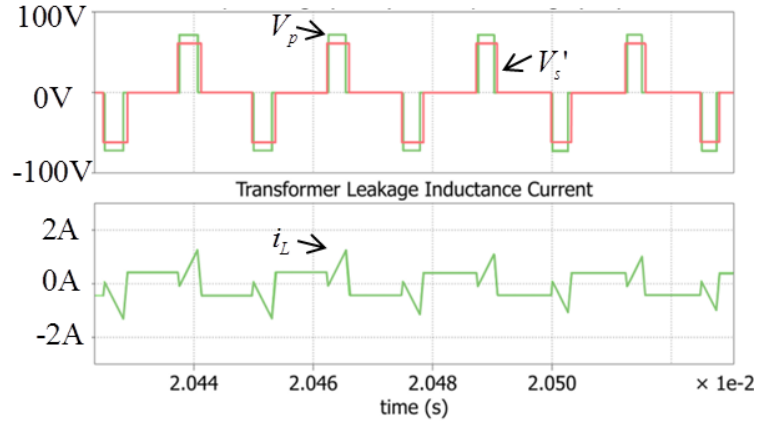
Fig. 4.3 Simulation Results of DAB Converter with PSM Control

4.3.2 Simulation with PWM Control

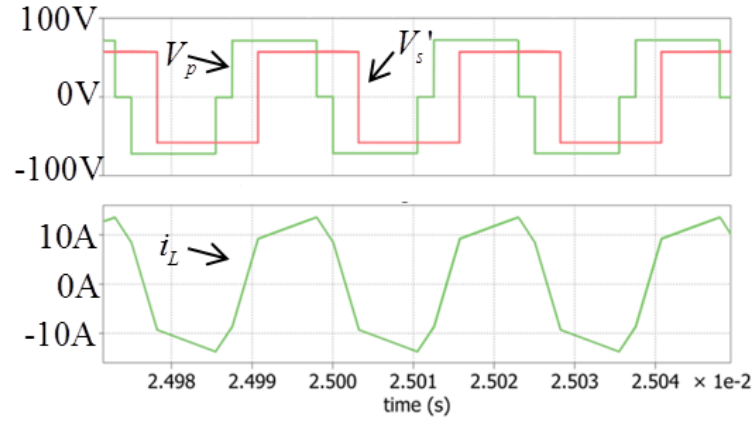
Fig. 4.4(a) shows the transformer leakage inductor current waveforms while Fig. 4.4(b) and 4.4(c) show the operation waveforms of DAB with PWM control at light load and maximum load respectively. The measurement shows that leakage inductance rms current is 5.95A, which is less than the rms current under PSM control. The waveforms of load power, DAB processing power and power variation on DC link capacitor are shown in Fig. 4.4(d). It can be seen that, on the DC link capacitor, there is only a low frequency power ripple of about 10W though some high frequency power ripple is inevitable.



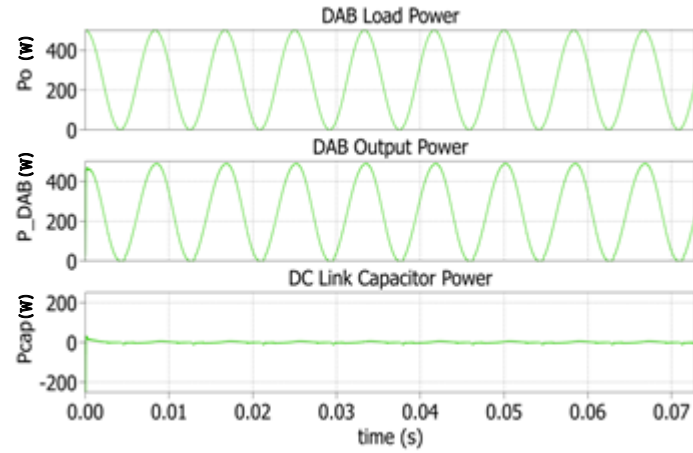
(a) Transformer Leakage Inductance Current with PWM Control



(b) Operation Waveforms of DAB with PWM Control at Light Load



(c) Operation Waveforms of DAB with PWM Control at Heavy Load



(d) DAB Load Power, Output Power and DC link Capacitor Power

Fig. 4.4 Simulation Results of DAB with PWM control

4.4 Experiment Verification

A DAB converter prototype with the same specifications as in simulation design is built for preliminary verification of the effect of PWM control.

4.4.1 DAB Converter Power Stage Design

As shown in Fig. 4.5, the power stage of DAB converter consists of two DC-AC H-bridge converters and a high-frequency transformer. One eZdsp™ F28335 evaluation board based control system is used to sample DAB converter input and output voltages, realize controller and provide gate signals for two H bridges.

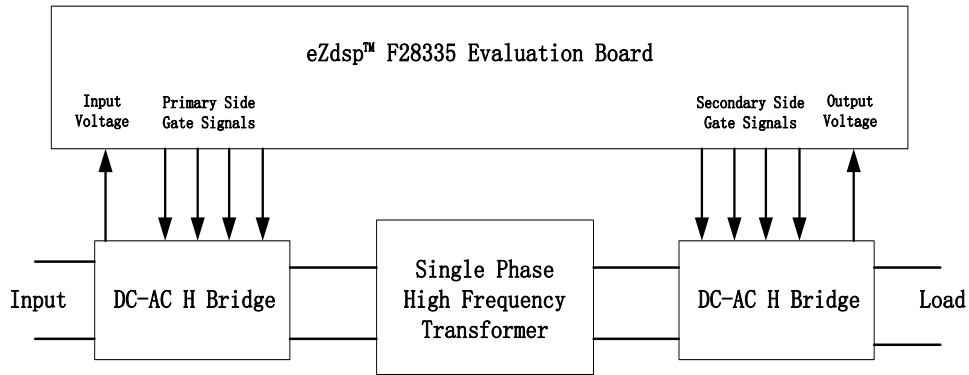


Fig. 4.5 DAB Converter Diagram

Considering the switch rated voltage and current, the Infineon IPP60R280C6 MOSFET is selected as switches for both input and output bridges. The DC link capacitors for both input and output sides are chosen as 60 μ F, consists of a 40 μ F and a 20 μ F EPCOS polypropylene film capacitors. In addition, one 47nF high-frequency response ceramic capacitor is added in both input and

output DC link capacitors. Fig. 4.6 shows the prototype of DAB converter without the connection of transform and inductor.

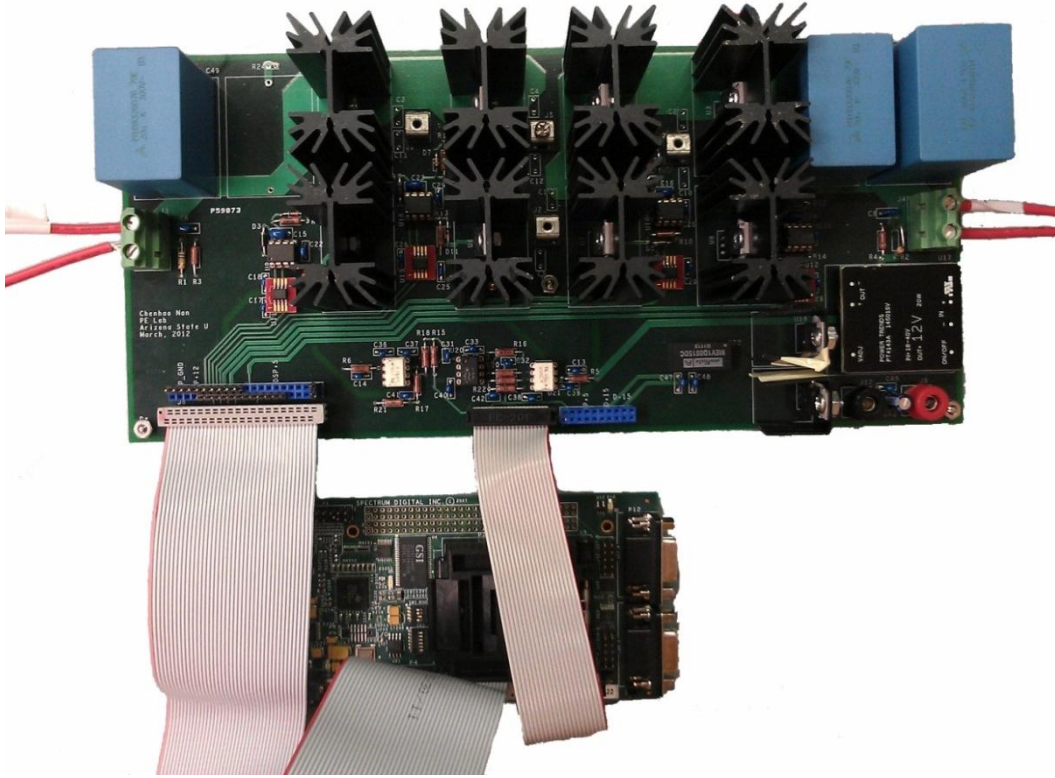


Fig. 4.6 Prototype of DAB Converter without Transformer and Inductor

4.4.2 High-frequency Transformer and Inductor Design

4.4.2.1 Transformer Design

From the previous analysis in Chapter 2 and Chapter 3, no matter what d value is, the volt-second of transformer with traditional PSM control is greater than that with PWM control. Considering the prototype converter will also run with PSM control for efficiency comparison, the transformer is designed based on

the volt-second in PSM control at maximum load, which is 500W from design specifications.

From Section 2.3, the maximum volt-second of the transformer is

$$\text{volt-second}_{\max} = \frac{\max\{V_i, V_o'\}}{2} \cdot T_s$$

And consequently the transformer apparent power is

$$P_t = \max\{V_i, V_o'\} \cdot I_{Lrms} = V_{\max} \cdot I_{Lrms} = 72V \times 10.5A = 756VA$$

where 10.5A is the leakage inductance rms current at 500W, determined from simulation with traditional PSM control.

Regarding to the transformer core material, soft ferrite is chosen due to its high frequency and cost-effective feature. Specifically, Ferroxcube 3C94 MnZn type ferrite is selected.

Regarding the winding material, litz wire is selected due to its high performance at high frequency. Based on the operation frequency 40kHz, the size of the single strand within litz wire is 36 AWG. Considering the available litz wire in the lab, the type with 265 strands of 36 AWG is used and thus from the data sheet of this litz wire, the conductor cross section area $A_{w(B)}$ is 3.357mm^2 .

Consequently, the maximum current density is

$$J_m = \frac{I_{Lrms}}{A_{w(B)}} = \frac{10.5A}{3.357\text{mm}^2} = 3.128A/\text{mm}^2$$

Initially assume the maximum operation flux density B_{\max} is 0.1T, the utilization factor k_u is 0.3 and the maximum current density J_m is 3.128A/mm², therefore

$$A_p = \frac{P_t}{k_u \cdot B_{\max} \cdot J_m \cdot f_{sw}} = \frac{756\text{VA}}{0.3 \times 0.1\text{T} \times 3.128\text{A/mm}^2 \times 40000\text{Hz}} = 201400\text{mm}^4$$

Thus Ferroxcube E65/32/27 core is chosen and its geometry parameters are shown in Table 4-2. Then the maximum operating flux density is updated as

$$B_{\max} = \frac{P_t}{k_u \cdot A_p \cdot J_m \cdot f_{sw}} = \frac{756\text{VA}}{0.3 \times 213000\text{mm}^4 \times 3.128\text{A/mm}^2 \times 40000\text{Hz}} = 0.094\text{T}$$

Table 4.2 E65/32/27 Core Geometry Parameters

E65/32/27		
Symbol	Parameter	Value
A_c	cross-sectional core area	540mm ²
W_a	window(winding) area	394mm ²
A_p	area product	213000mm ⁴
MLT	mean length per turn	150mm

The number of turns of primary winding is

$$N_{pri} = \frac{V_{\max}/2}{A_c \cdot B_{\max} \cdot f_{sw}} = \frac{36\text{V}}{540\text{mm}^2 \times 0.094\text{T} \times 40000\text{Hz}} = 17.61 \approx 18 \text{ turns}$$

and from the 1:1 turns ratio,

$$N_{sec} = N_{pri} = 18 \text{ turns}$$

Then k_u is verified as

$$k_u = \frac{A_{w(B)} \cdot N_{pri} + A_{w(B)} \cdot N_{sec}}{W_a} = \frac{3.357\text{mm}^2 \times (18+18)}{394\text{mm}^2} = 0.306 \approx 0.3$$

The measurement of the built transformer, as shown in Fig. 4.7, shows the leakage inductance is $9\mu\text{H}$.

4.4.2.2 Inductor Design

Based on the converter design, the total leakage inductance is supposed to be $23.3\mu\text{H}$. The leakage inductance of transformer is only $9\mu\text{H}$ and therefore an extra external inductor of $14.3\mu\text{H}$ is needed.

The design of the inductor is still based on the maximum power with traditional PSM control. From the simulation, the maximum and rms values of leakage inductance current are 13.28A and 10.5A respectively.

The same litz wire, as used in the transformer, is selected here and therefore the current density is the same as that in transformer,

$$J_m = \frac{I_{Lrms}}{A_{w(B)}} = \frac{10.5\text{A}}{3.357\text{mm}^2} = 3.128\text{A/mm}^2$$

Then assume utilization factor k_u is 0.3, maximum flux density B_{\max} is 0.15T ,

$$A_p = \frac{L \cdot I_{Lpk} \cdot I_{Lrms}}{k_u \cdot B_{\max} \cdot J_m} = \frac{9\mu\text{H} \times 13.28\text{A} \times 10.5\text{A}}{0.3 \times 0.15\text{T} \times 3.128\text{A/mm}^2} = 14364\text{mm}^4$$

Thus the closest commercial core Ferroxcube E41/17/12 is selected. The geometry parameters of E41/17/12 are shown below in Table 4-3. Then the new operating maximum flux density is

$$B_{\max} = \frac{L \cdot I_{Lpk} \cdot I_{Lrms}}{k_u \cdot A_p \cdot J_m} = \frac{9\mu\text{H} \times 13.28\text{A} \times 10.5\text{A}}{0.3 \times 17900\text{mm}^4 \times 3.128\text{A/mm}^2 \times 40000\text{Hz}} = 0.12\text{T}$$

Table 4.3 E41/17/12 Core Geometry Parameters

E41/17/12		
Symbol	Parameter	Value
A_c	cross-sectional core area	149mm^2
W_a	window(winding) area	120mm^2
A_p	area product	17900mm^4
MLT	mean length per turn	79.6mm

Thus the number of turns is

$$N = \frac{L \cdot I_{Lpk}}{A_c \cdot B_{\max}} = \frac{9\mu\text{H} \times 13.28\text{A}}{149\text{mm}^2 \times 0.12\text{T}} = 10.76 \approx 11$$

Then the utilization factor is verified as

$$k_u = \frac{A_{w(B)} \cdot N}{W_a} = \frac{3.357\text{mm}^2 \times 11}{120\text{mm}^2} = 0.307 \approx 0.3$$

The air-gap of the inductor is determined by

$$l_g = \frac{\mu_0 \cdot N^2 \cdot A_c}{L} = \frac{0.4\pi \times 10^{-8} \text{H/m} \times 11^2 \times 149\text{mm}^2}{9\mu\text{H}} = 1.618\text{mm}$$

The built inductor is also shown in Fig. 4.9. The design parameters of the transformer and inductor are summarized in Table 4.4.

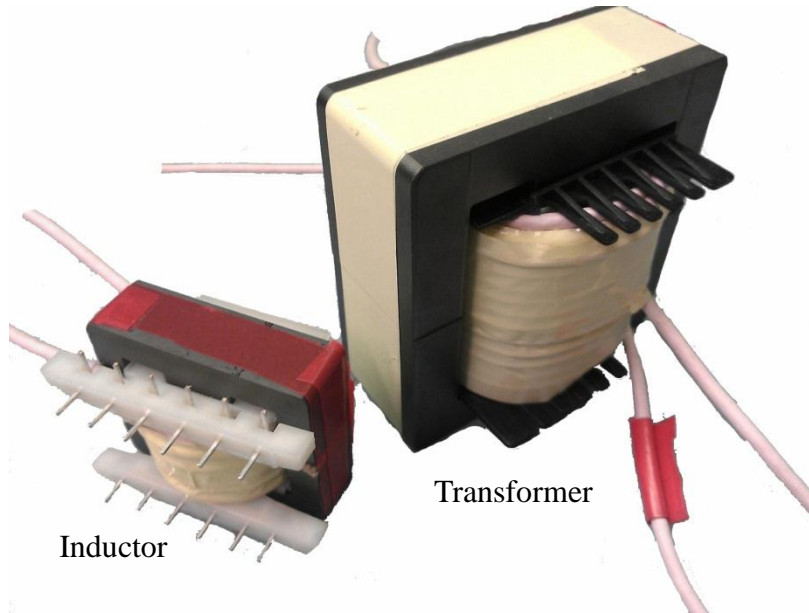


Fig. 4.7 DAB High Frequency Transformer and External Inductor

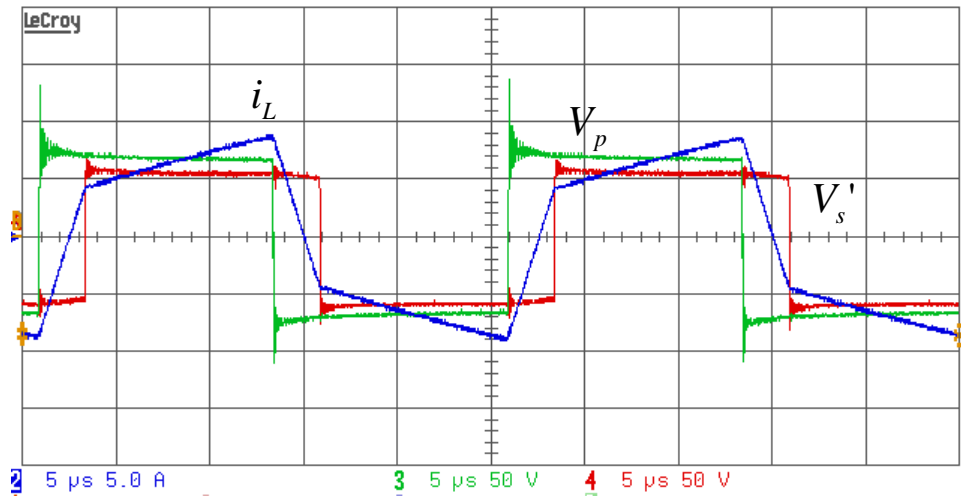
Table 4.4 Design Parameters of Transformer and Inductor

	Transformer	Inductor
Core Material	Ferroxcube 3C94 (Ferrite)	
Core Size	E65/32/27	E41/17/12
Winding	Litz Wire (265 strands of AWG 36)	
Number of Turns	$N_{pri}=N_{sec}=18$	$N=11$
Flux Density B_m	0.094T	0.12T
Current Density J_m	$3.128A/mm^2$	
Air Gap l_g	NA	1.168mm

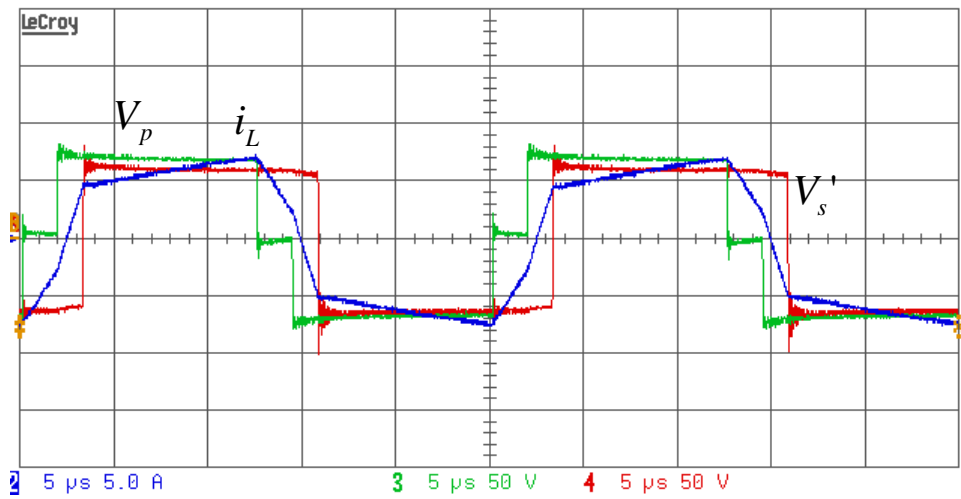
4.4.3 Prototype DAB Converter Test Results

4.4.3.1 Tests Results with DC Load

Fig. 4.8(a) shows the voltage and leakage inductance current waveforms of DAB with PSM control at a power level of 350W while Fig. 4.8(b) shows the operation waveforms of DAB at the same power level with PWM control. The measured transformer leakage inductance rms currents with PSM and PWM controls are 6.366 and 5.655 respectively. For the light load operation, Fig. 4.9(a) shows the voltage and leakage inductance current waveforms with PSM control at 100W and Fig. 4.9(b) shows the waveforms with PWM control at 100W as well. The measured transformer leakage inductance rms current reduces from 2.526A with PSM control to 2.205A with PWM control. In addition, it is clearly that with PSM control the output bridge is experiencing hard-switching due to the negative current value in the transition point.

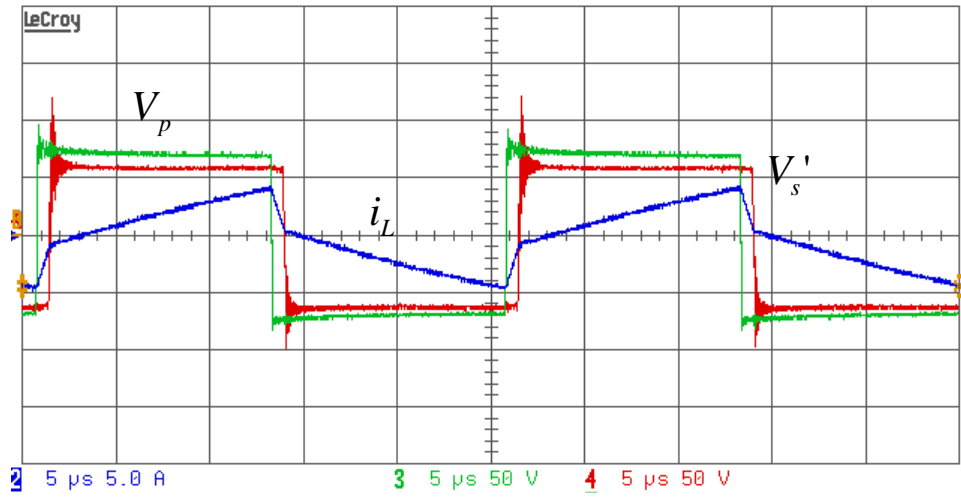


(a) PSM Control

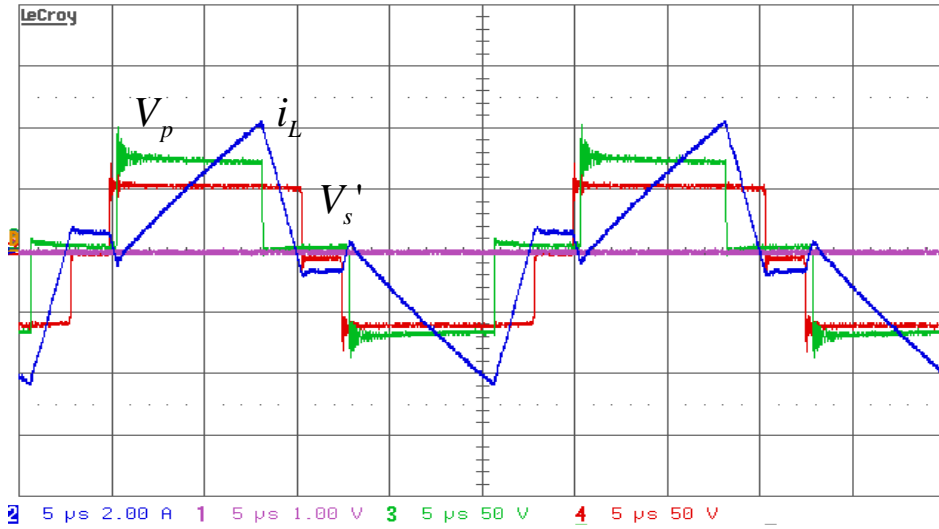


(b) PWM Control

Fig. 4.8 Experiment Results at Heavy Load with PSM and PWM control



(a) PSM Control



(b) PWM Control

Fig. 4.9 Experiment Results at Light Load with PSM and PWM control

To further compare the rms current and the conversion efficiency, the data of more operating points is measured and the efficiency comparison between PSM and PWM control is shown in Fig. 4.10. It is obviously that the DAB converter efficiency with PWM control is much better than the efficiency with PSM control

at light load. For the heavy load, the efficiency with PWM control is still higher though not significant than that with PSM control. Not very high peak efficiency is reasonable in this experiment due to the large conduction losses caused by large on-state resistance of the used MOSFET.

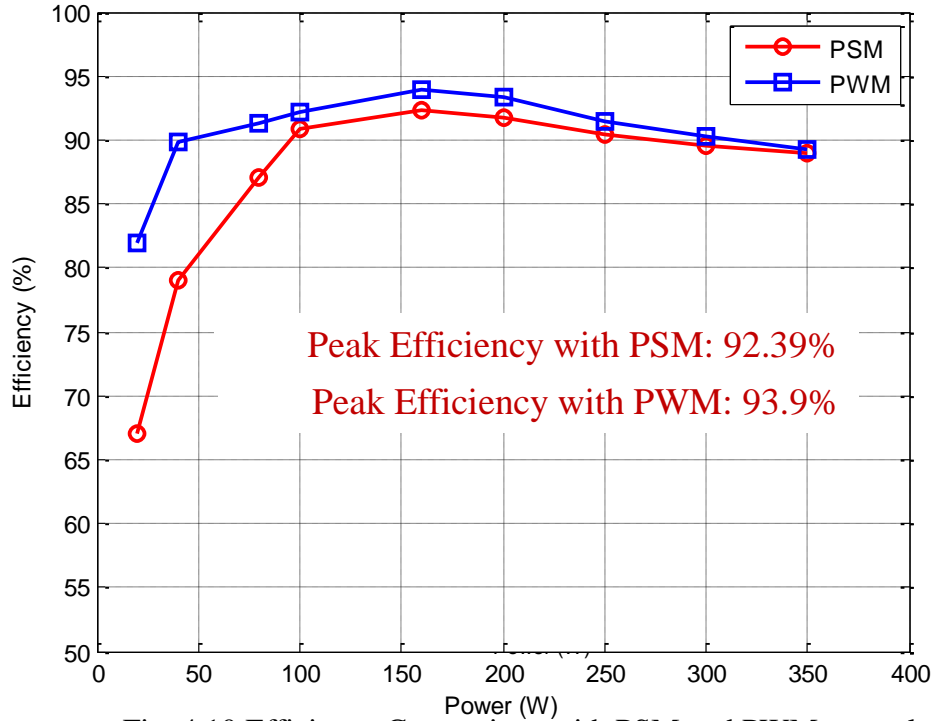


Fig. 4.10 Efficiency Comparison with PSM and PWM control

4.4.3.2 Tests Results with AC Load

The AC Load is realized by an inverter working in the stand alone mode that followed by four 10Ω power resistors paralleled. The whole system setup is shown in Fig. 4.11. Fig. 4.12 shows the transformer leakage inductance current and inverter output voltage. The DAB input current is shown in Fig. 4.13. It is measured that the input current rms value is 3.59A and, with the input voltage of

72V, the input power is calculated as 258.5W. Regarding to the load, the rms voltage of the inverter output is 22V. Considering the 2.5Ω Load, the output power is 193.6W. Thus, the efficiency is

$$\frac{P_o}{P_{in}} = \frac{193.6W}{258.5W} = 74.89\%$$

However it should be noted that the load inverter rated power is 4kW and thus the conversion efficiency at light load could be very low. If we assume the inverter efficiency is 85%, then the DAB converter efficiency is 88.1% which is comparable with the efficiency of DAB operated at constant power.

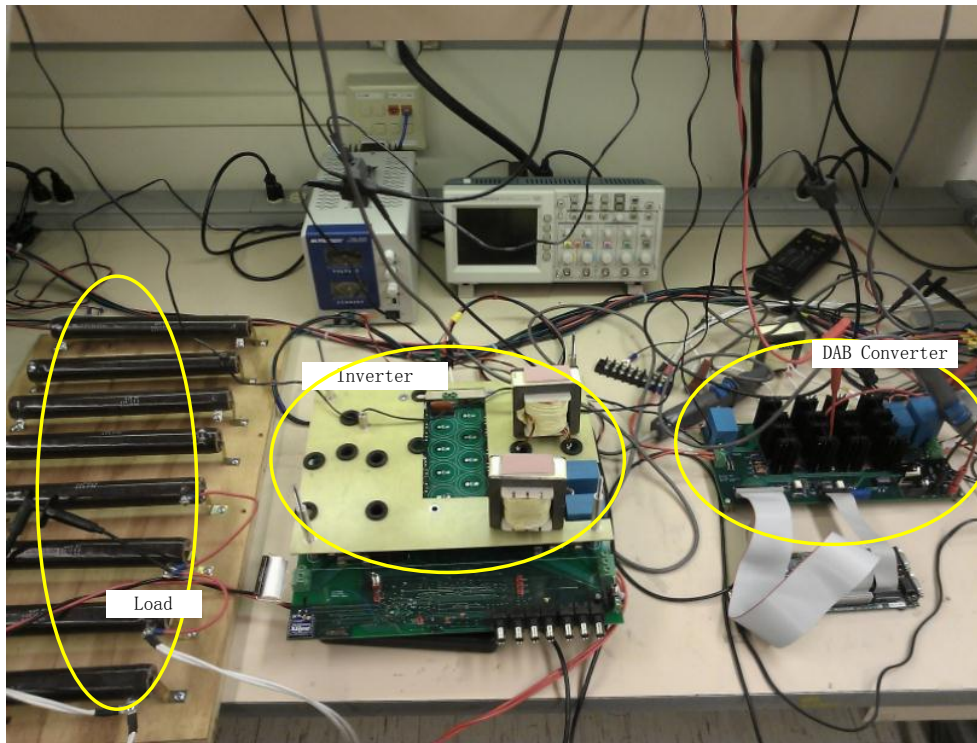


Fig. 4.11 Experiment System Setup

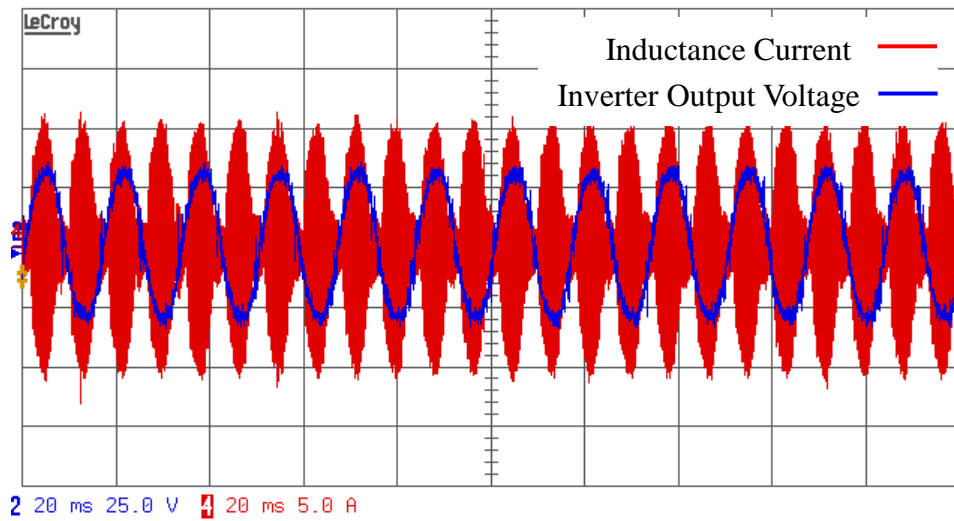


Fig. 4.12 Inverter Output Voltage and Transformer Leakage Inductance Current

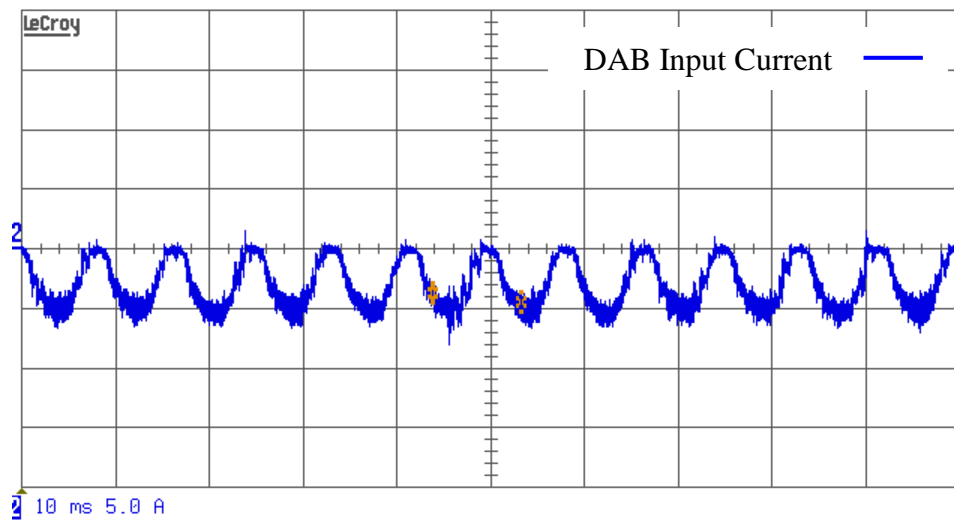


Fig. 4.13 DAB Converter Input Current

Chapter 5. Conclusion

This thesis has presented the basic analysis of DAB converter with traditional PSM control and analyzed the PWM control of DAB converter comprehensively. With the PWM control, theoretically, the DAB converter can extend the ZVS range down to zero load and minimize the rms current of transformer leakage inductance at light load; consequently, the conversion efficiency, especially at light load, is increased significantly. In addition, the apparent power of the transformer is reduced with the PWM control of DAB and therefore the size of the transformer is reduced. Furthermore, for the practical implementation of PWM control, the effect of the switch output capacitance is analyzed.

Then the PWM control is applied to reduce the DC link capacitors of DAB converter in a three-stage SST while achieving high conversion efficiency. The effect of using PWM control to the DC link capacitance is investigated. A 40kHz, 500W DAB converter is designed and then simulated in the PLECS verifying the effect of using PWM control of DAB. Finally, a 500W prototype DAB converter, including the high frequency transformer and the external leakage inductor, is built and the experiment results show that, with the PWM control, the output DC

link capacitor of DAB in the SST is reduced to $60\mu\text{F}$ while the efficiency is still comparable with that of DAB operated at constant rated power.

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